

PG150-C03

384b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

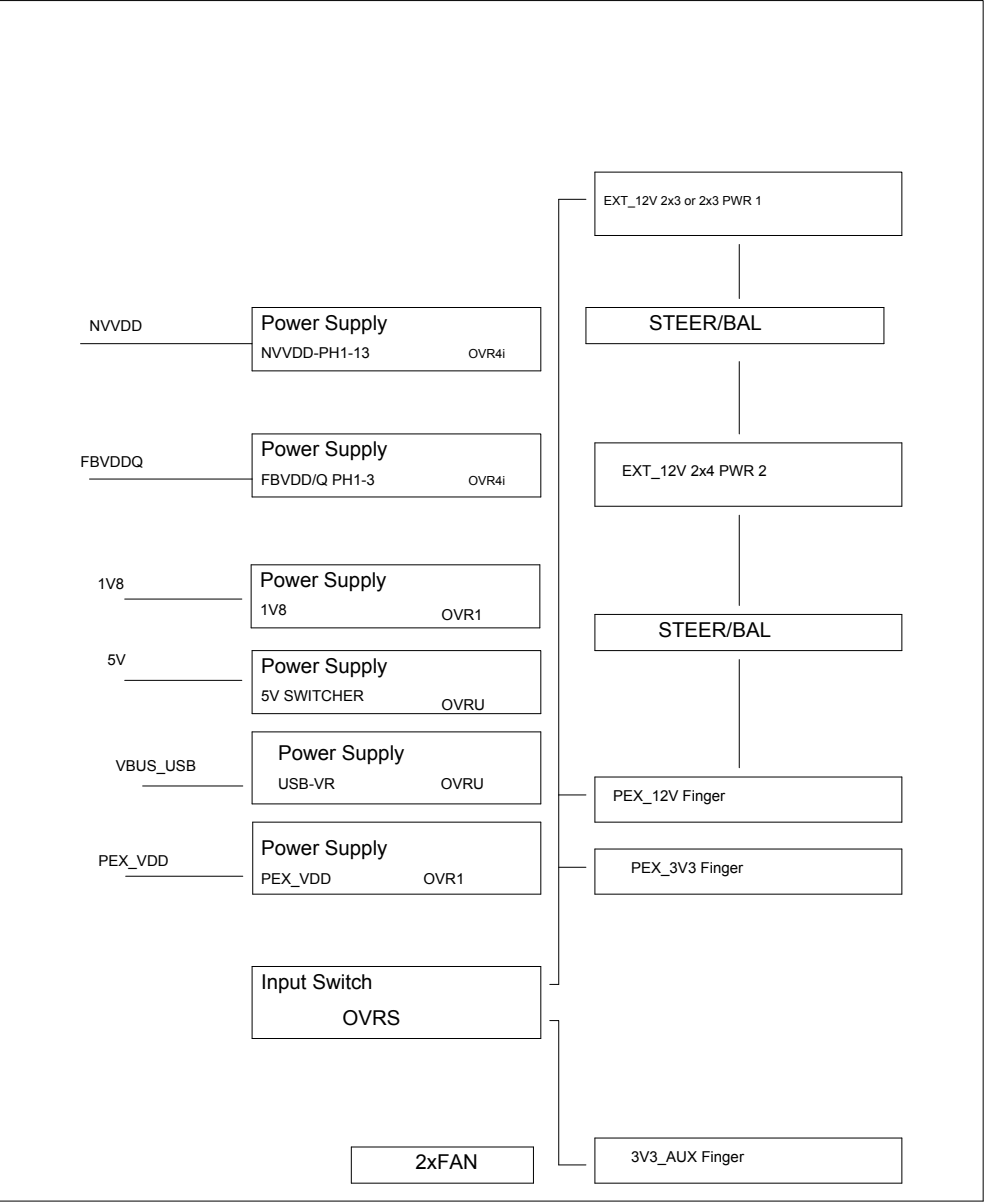
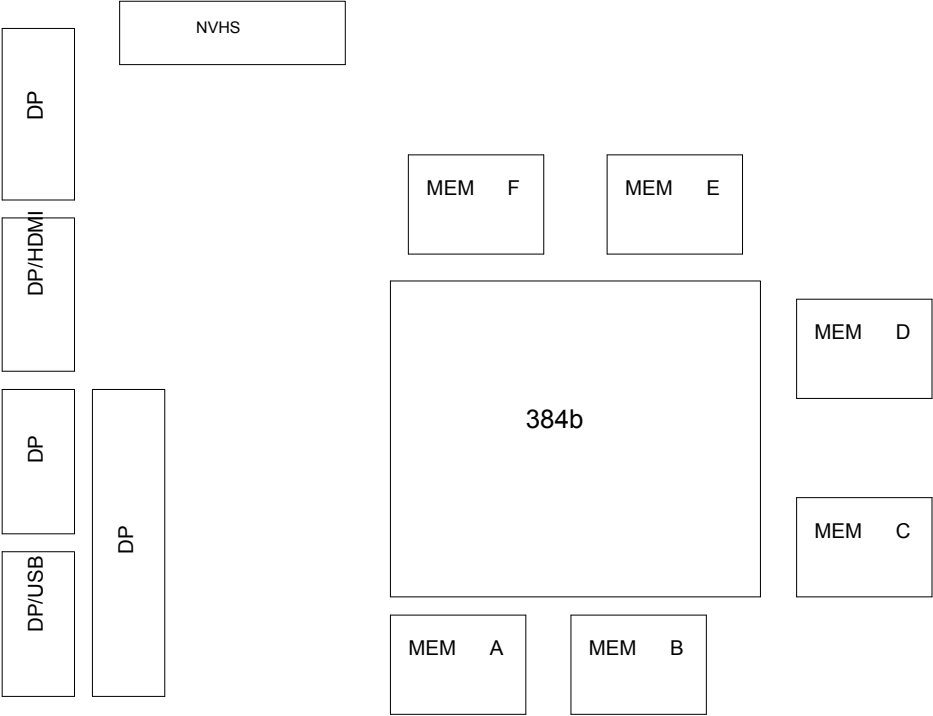
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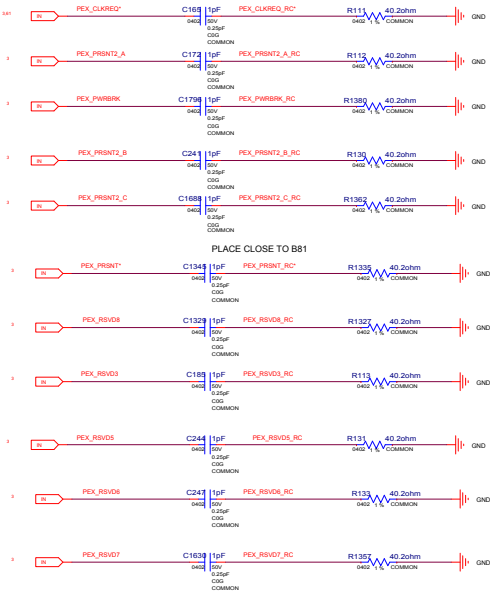
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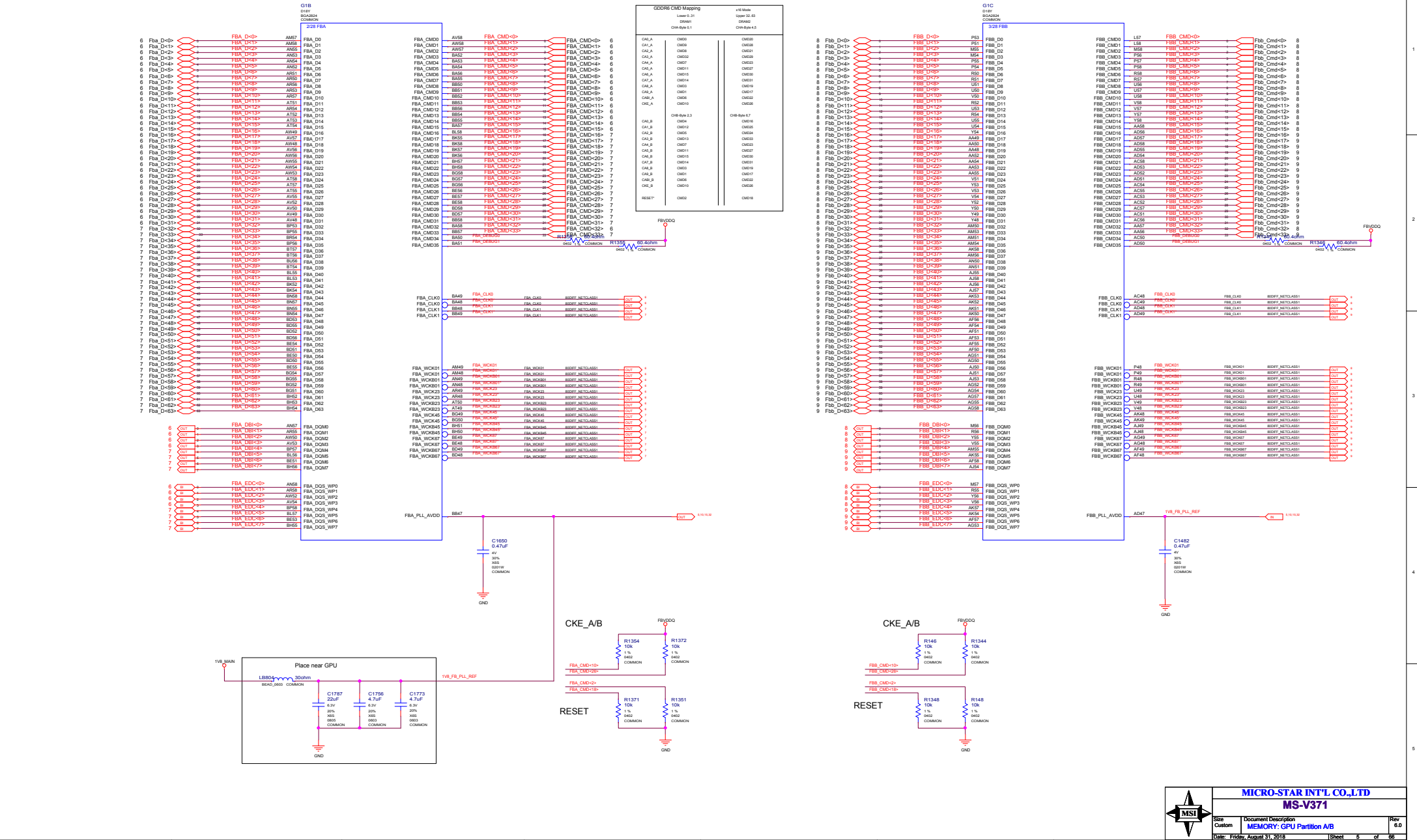
Block Diagram



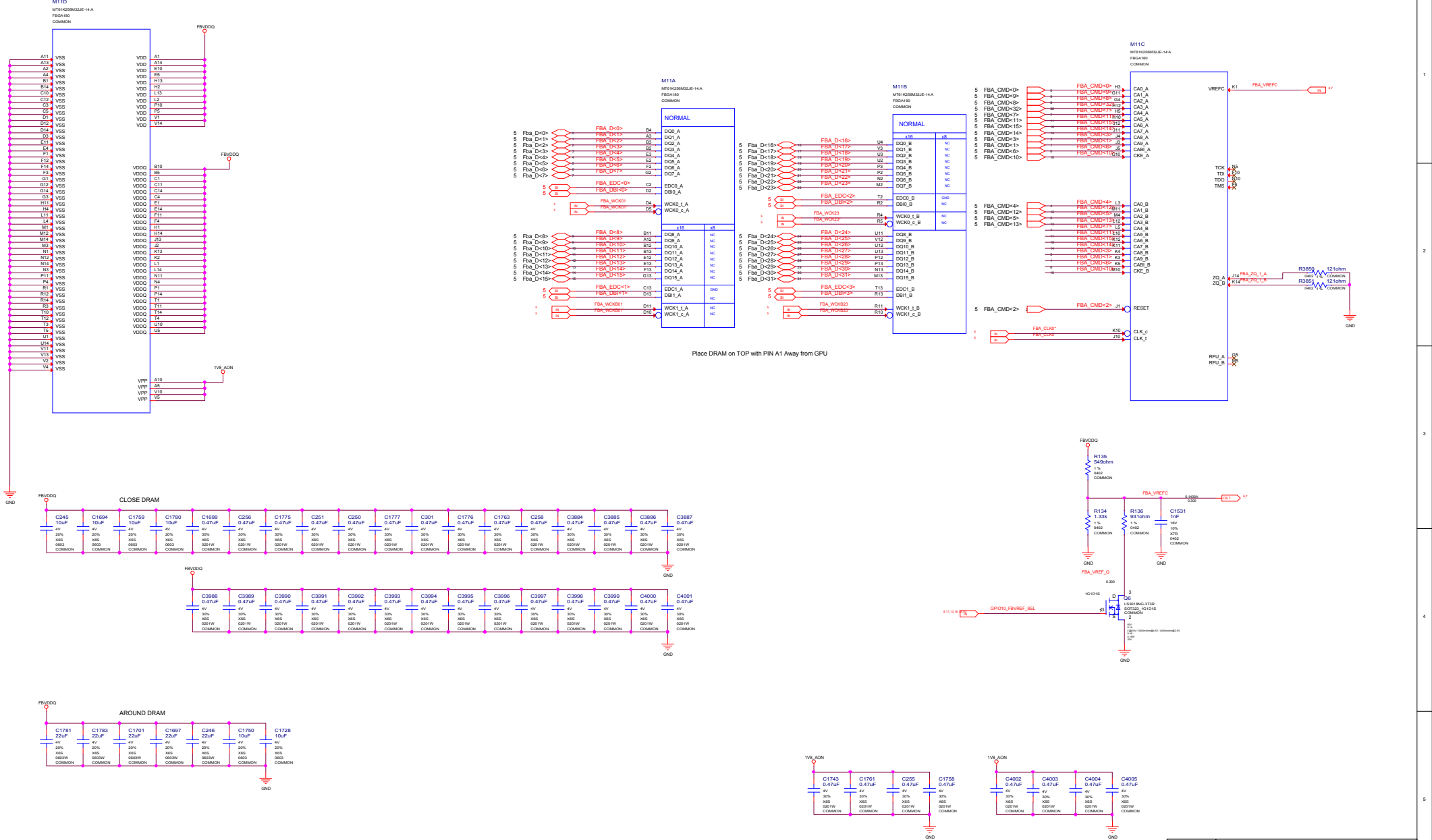
PCI TERM



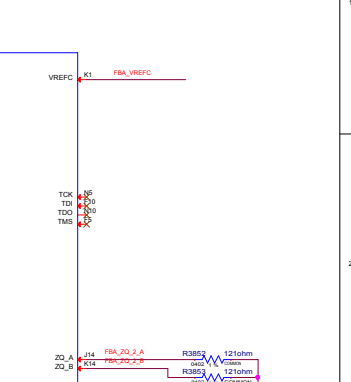
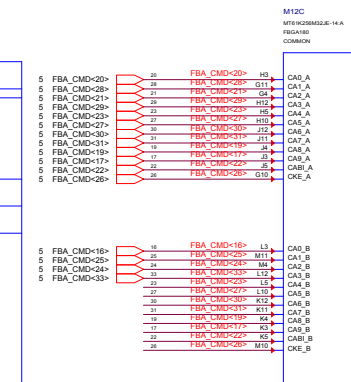
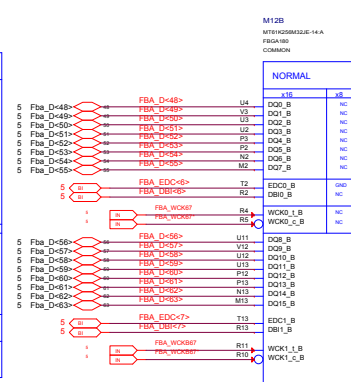
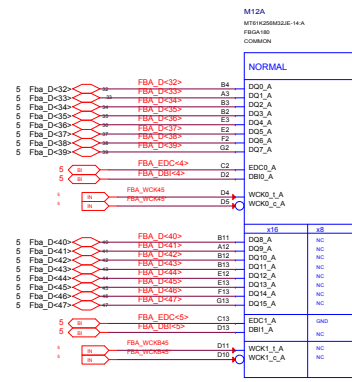
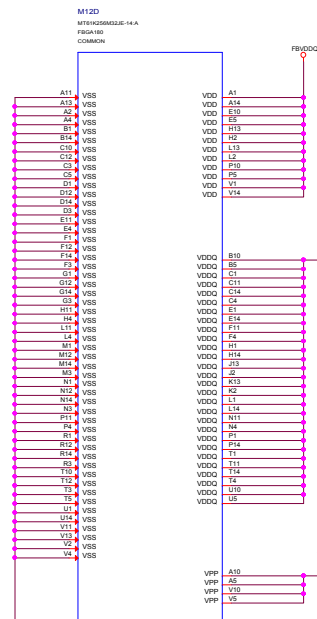
MEMORY: GPU Partition A/B



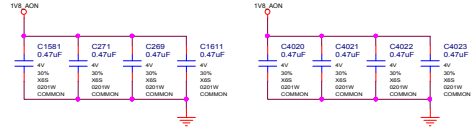
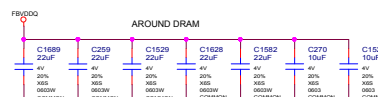
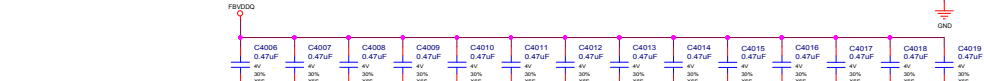
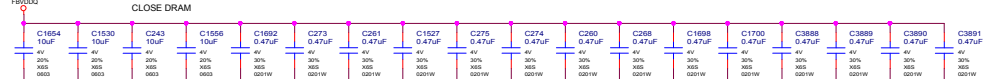
MEMORY: FBA Partition 31..0



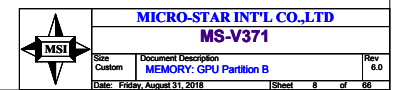
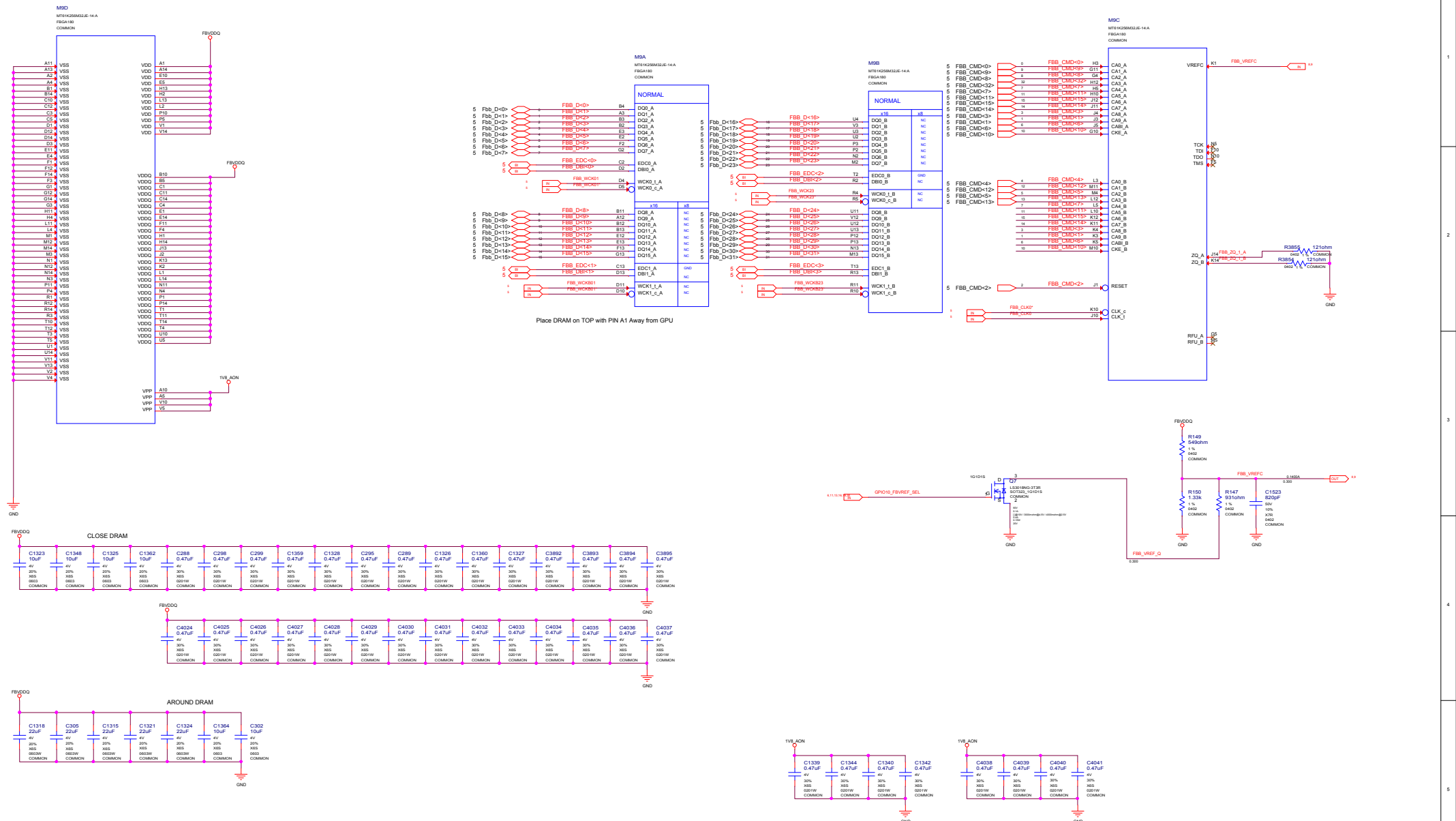
MEMORY: FBA Partition 63..32



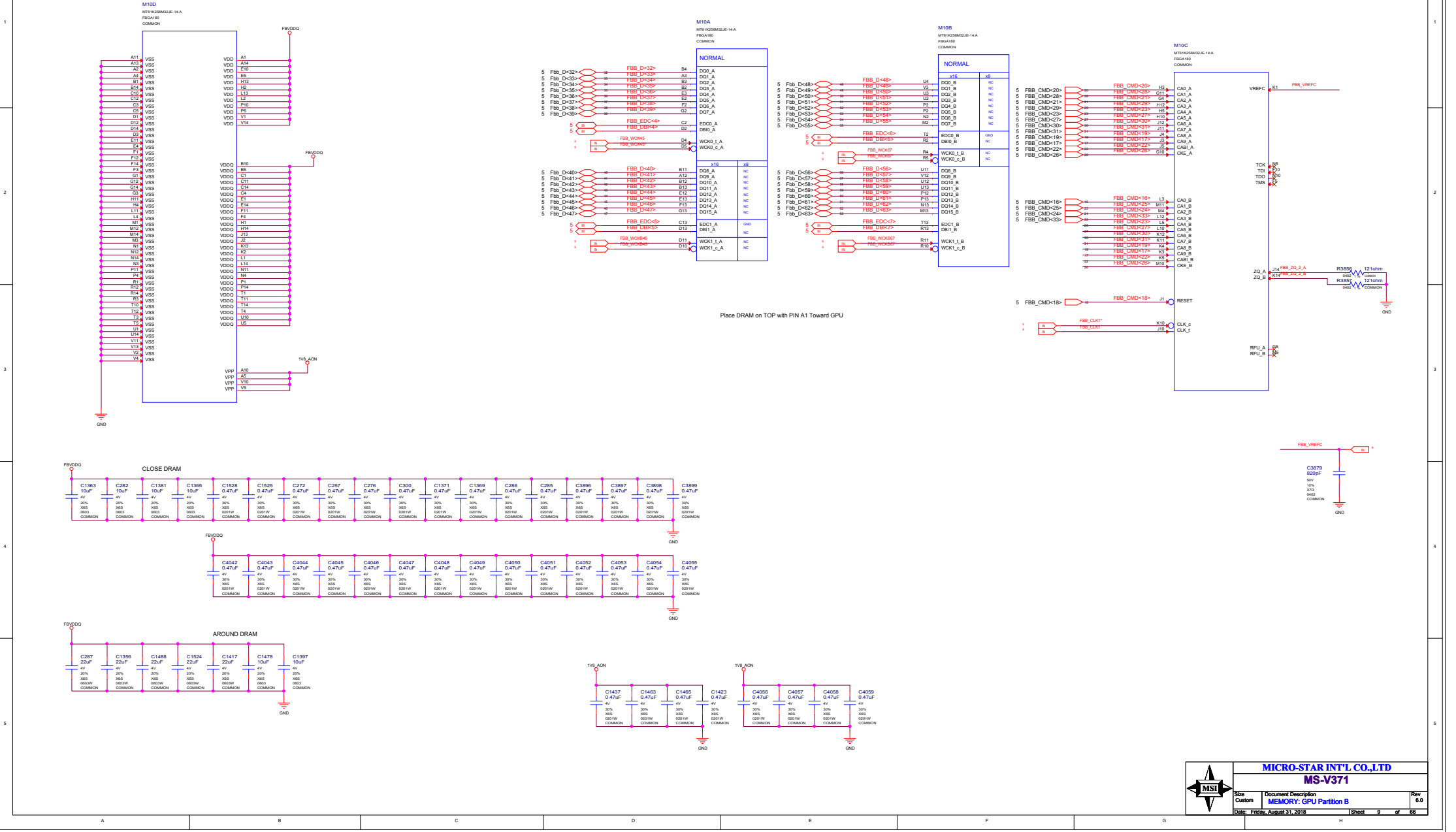
Place DRAM on TOP with PIN A1 Toward GPU



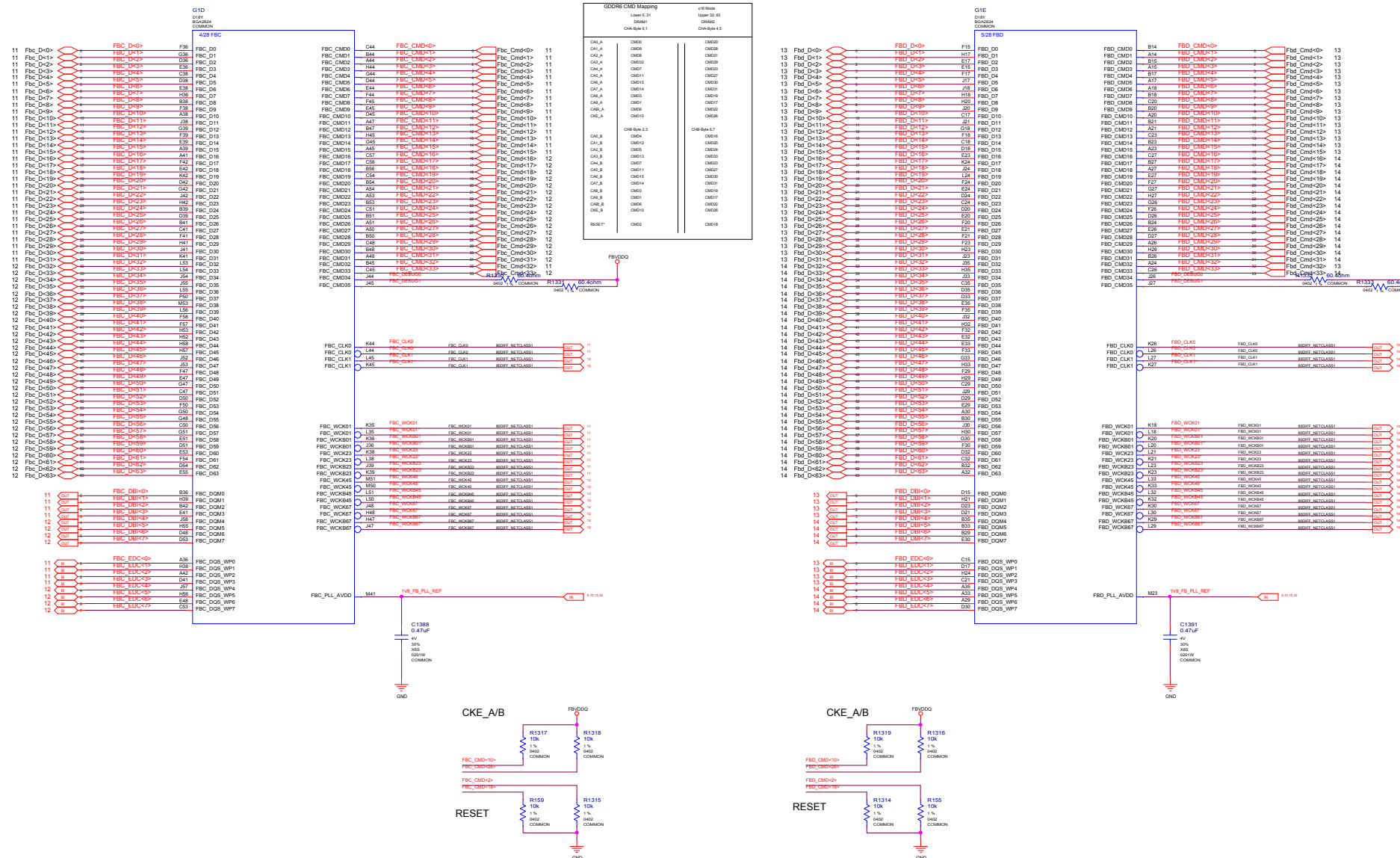
MEMORY: FBB Partition 31..0



MEMORY: FBB Partition 63..32



MEMORY: GPU Partition C/D

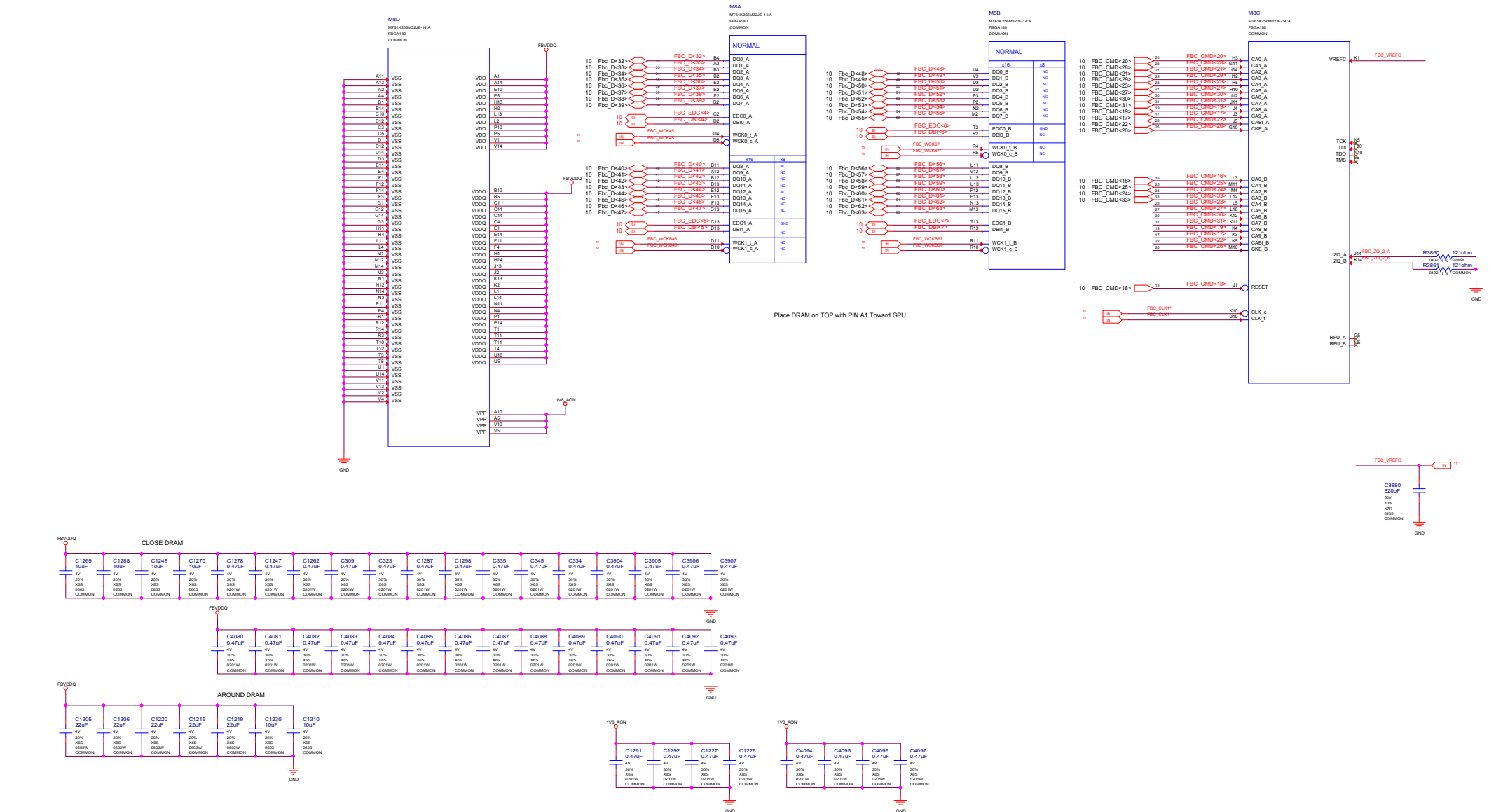


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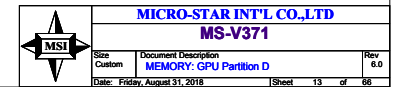
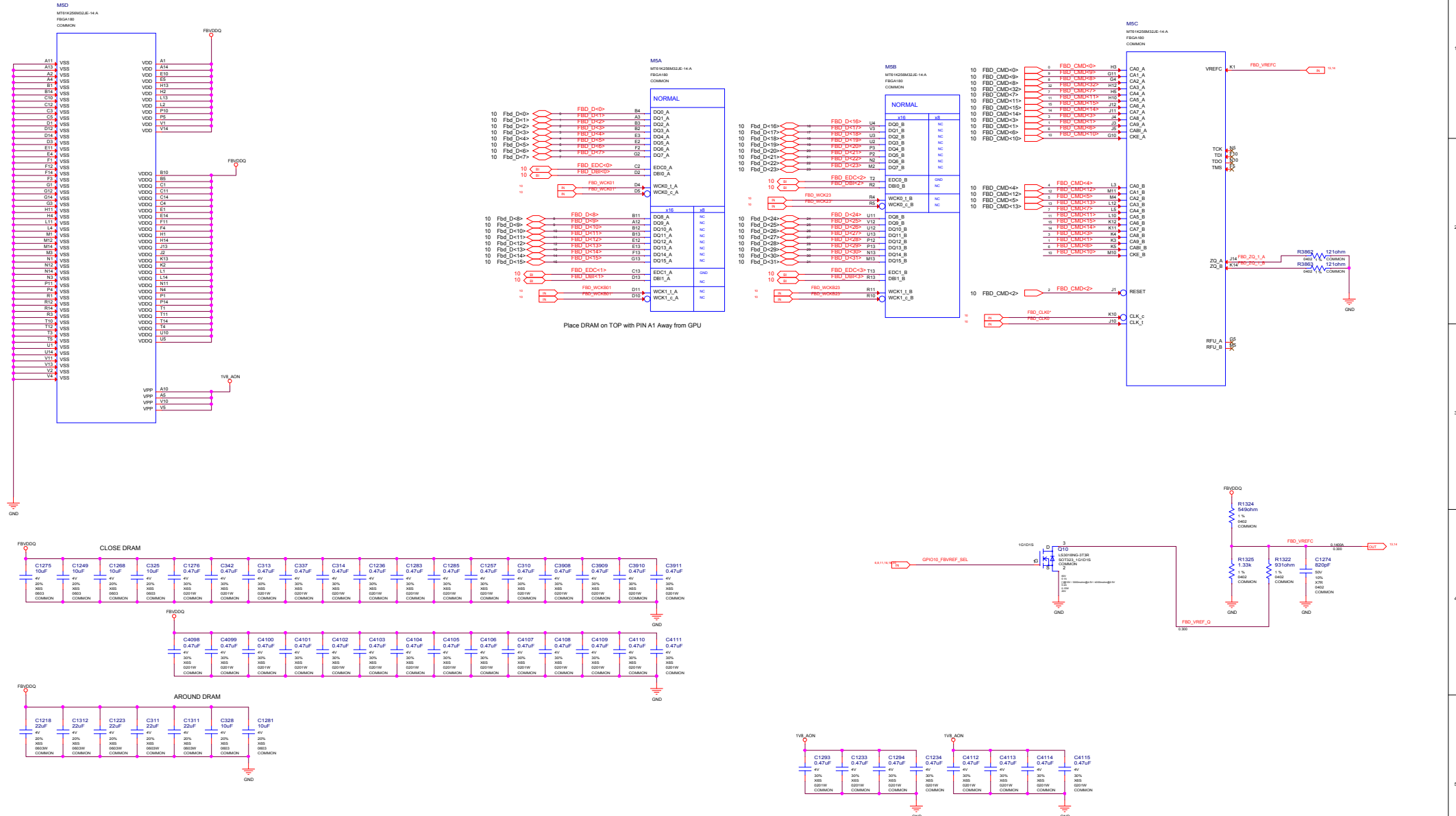
MS-V371

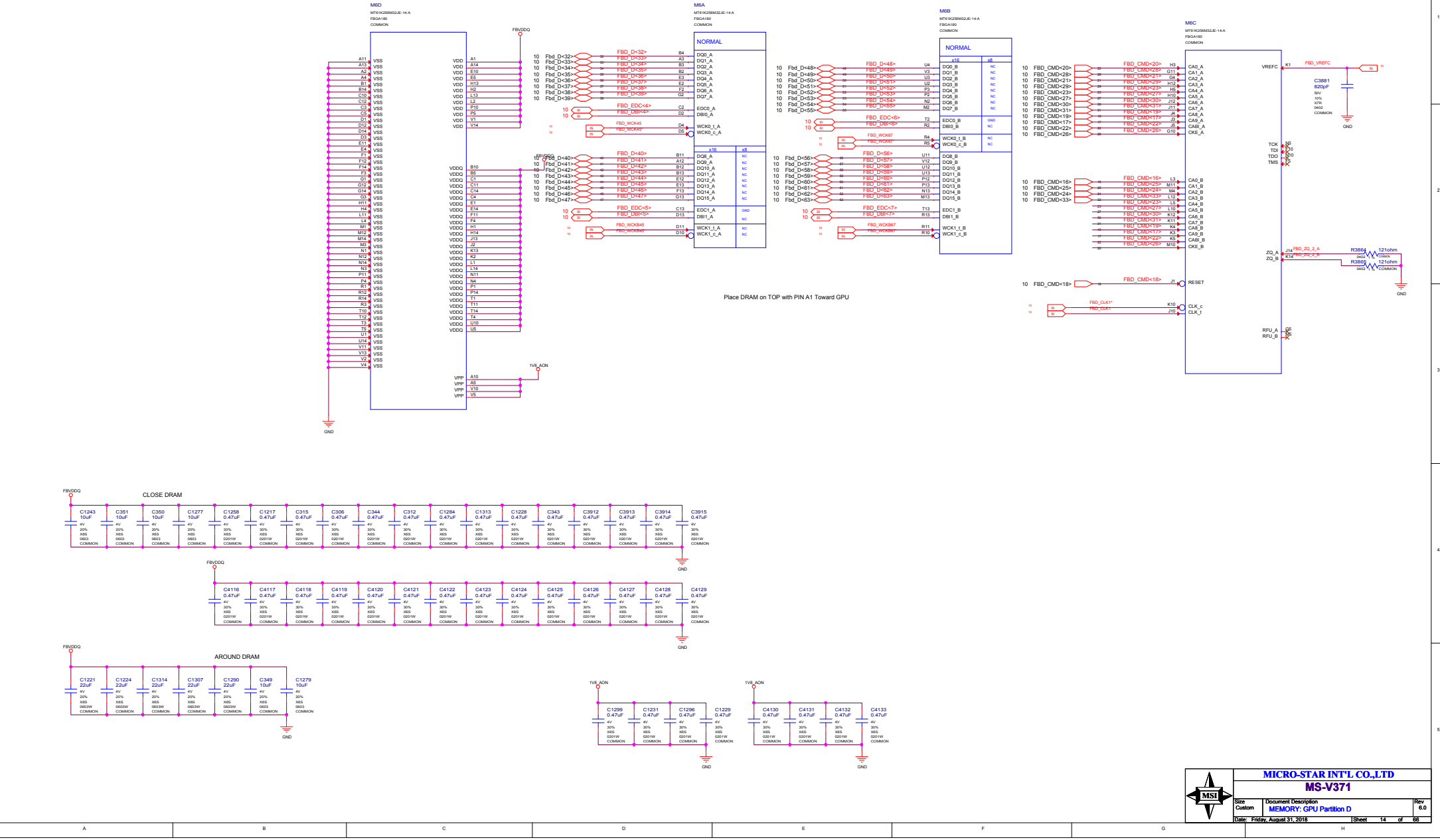
Size	Document Description	Rev
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Custom	MEMORY: GPU Partition C/D	6.0
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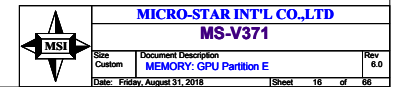
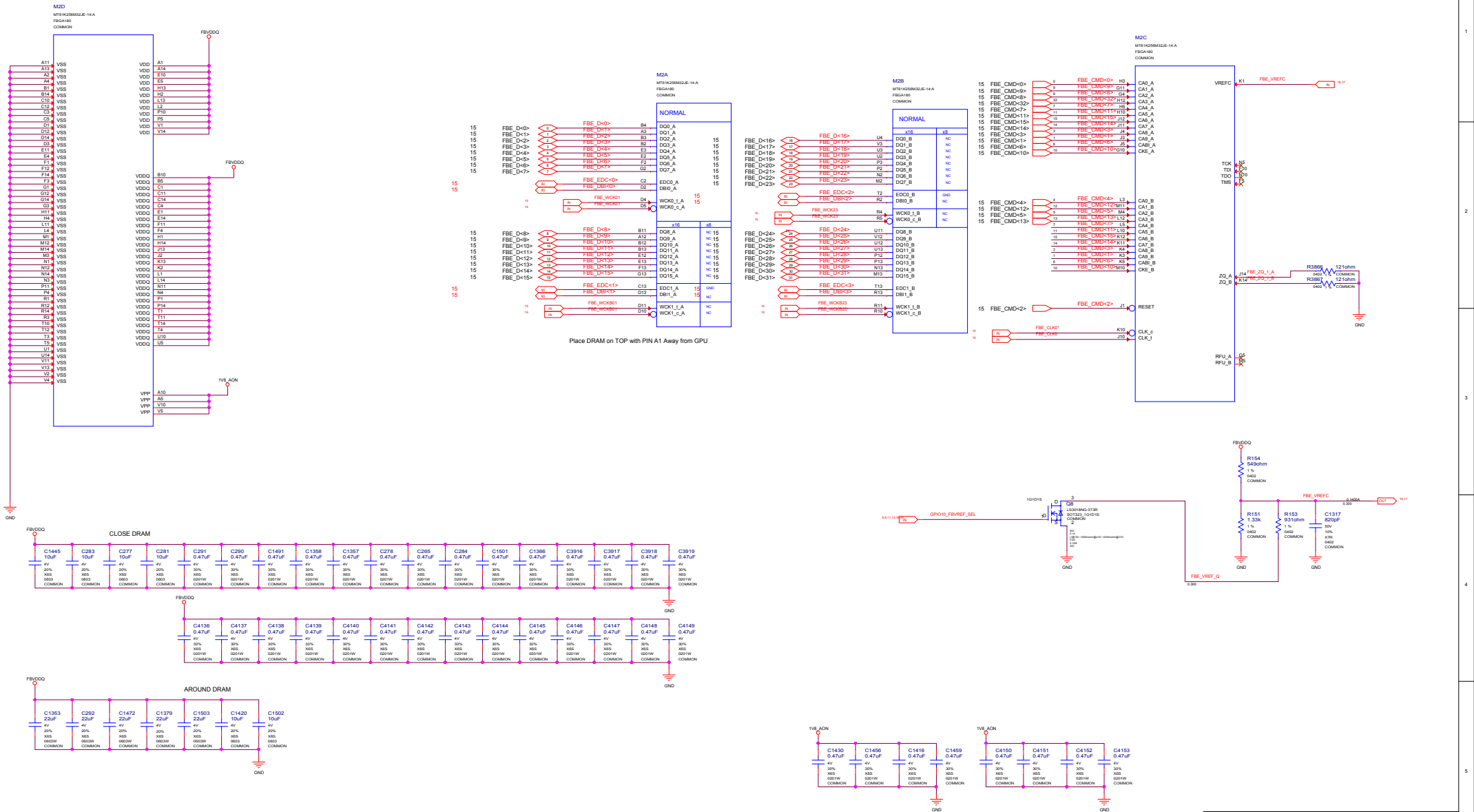


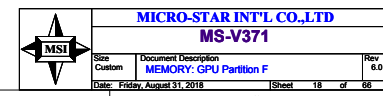
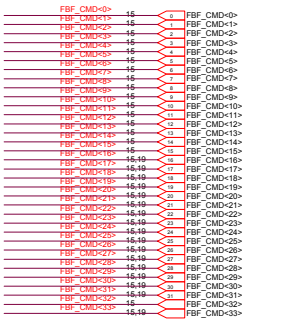
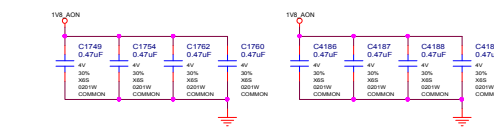
MEMORY: FBD Partition 31..0

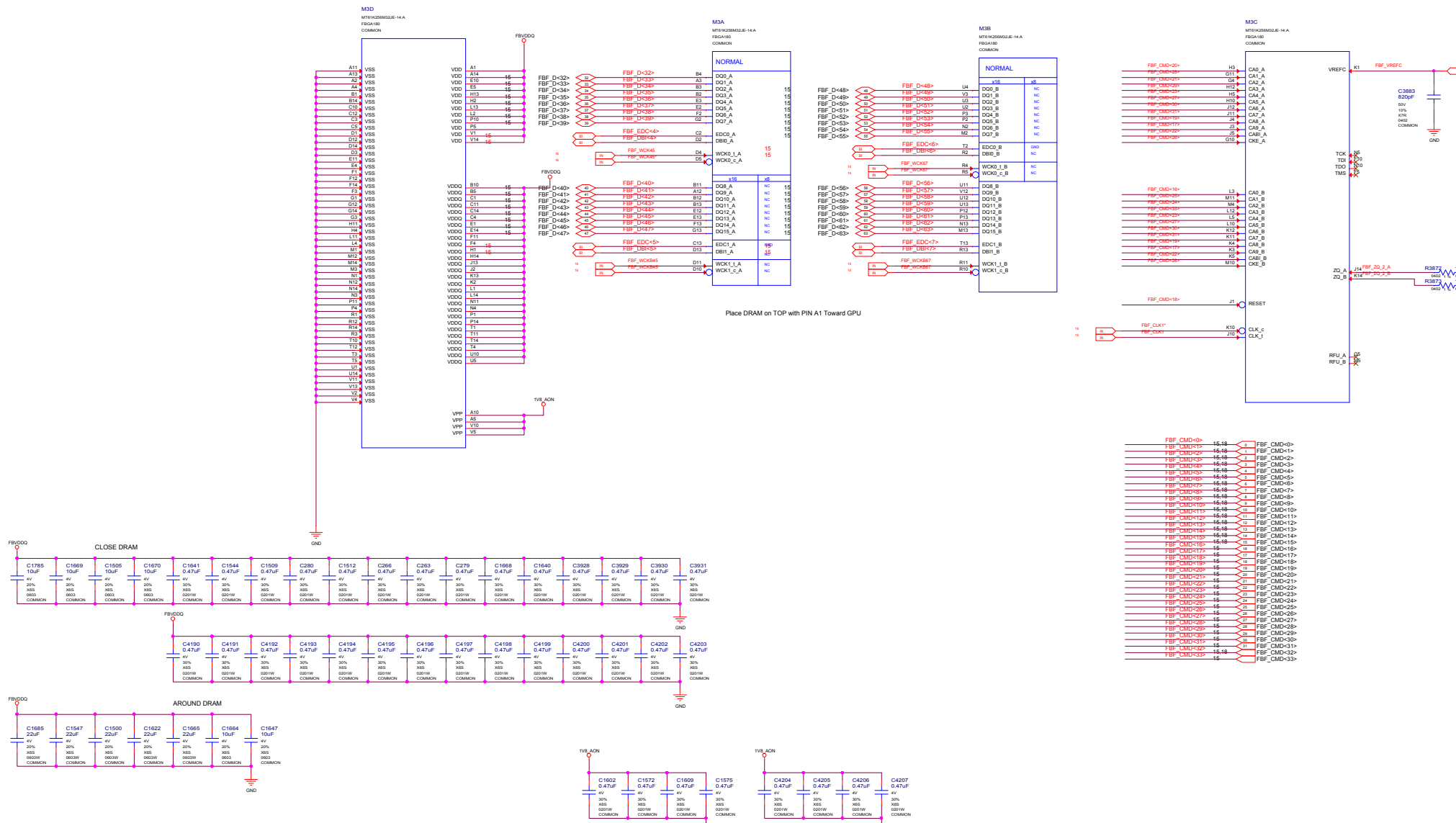




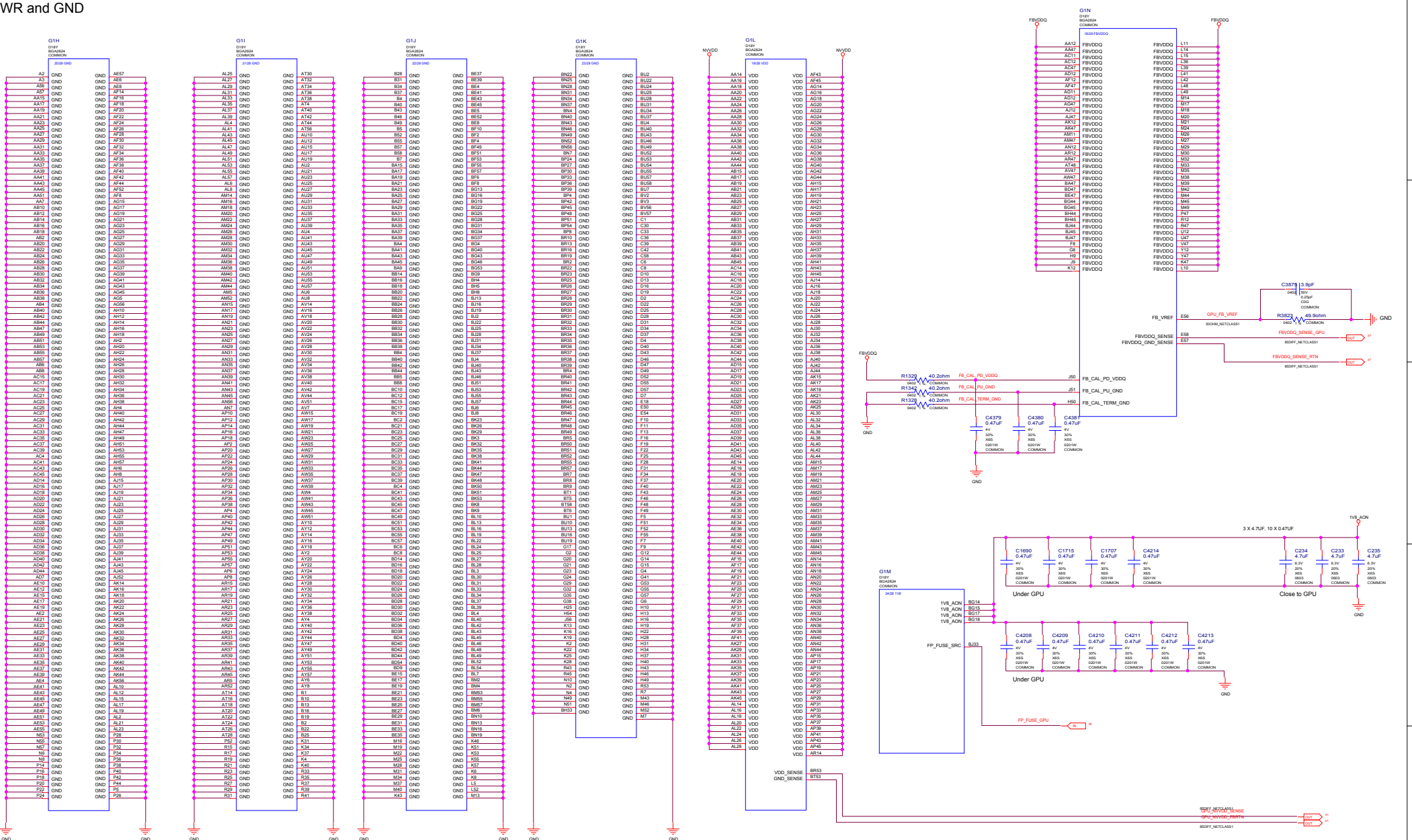
MEMORY: FBE Partition 31..0







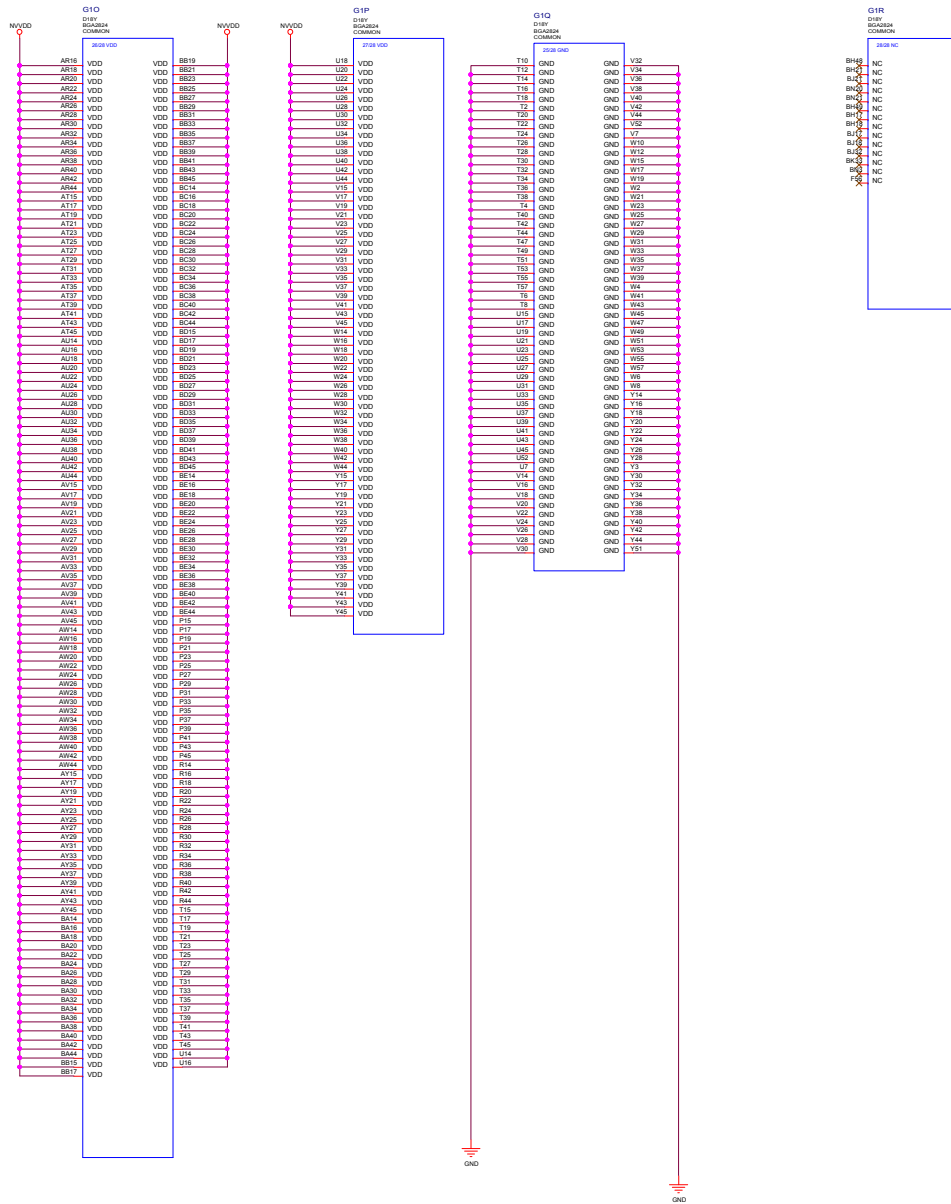
GPU PWR and GND



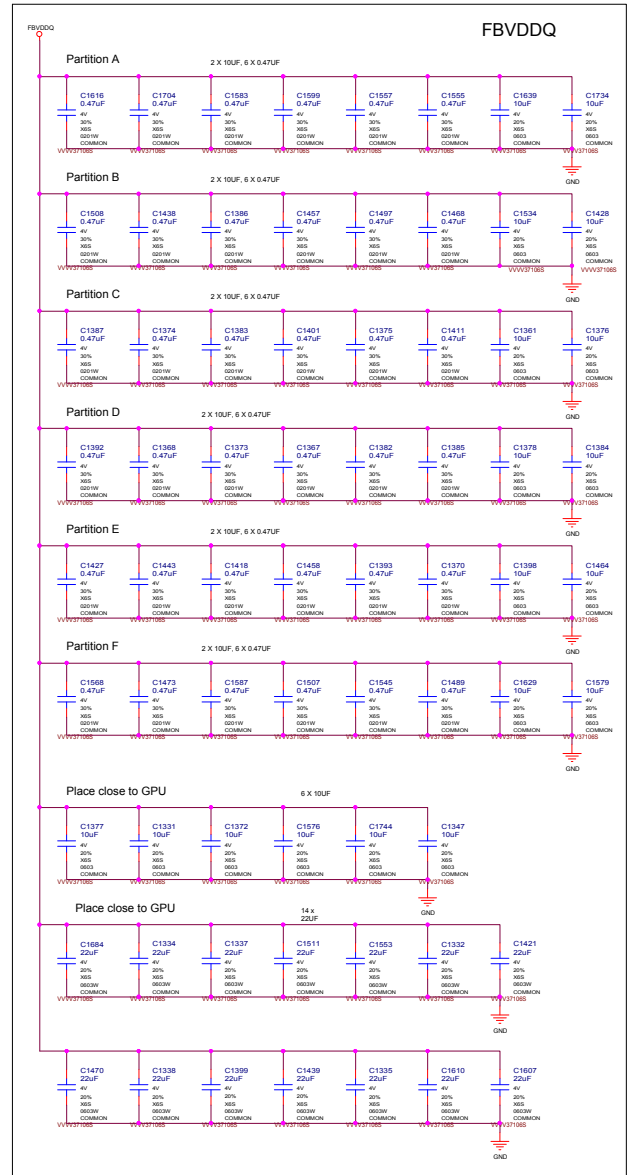
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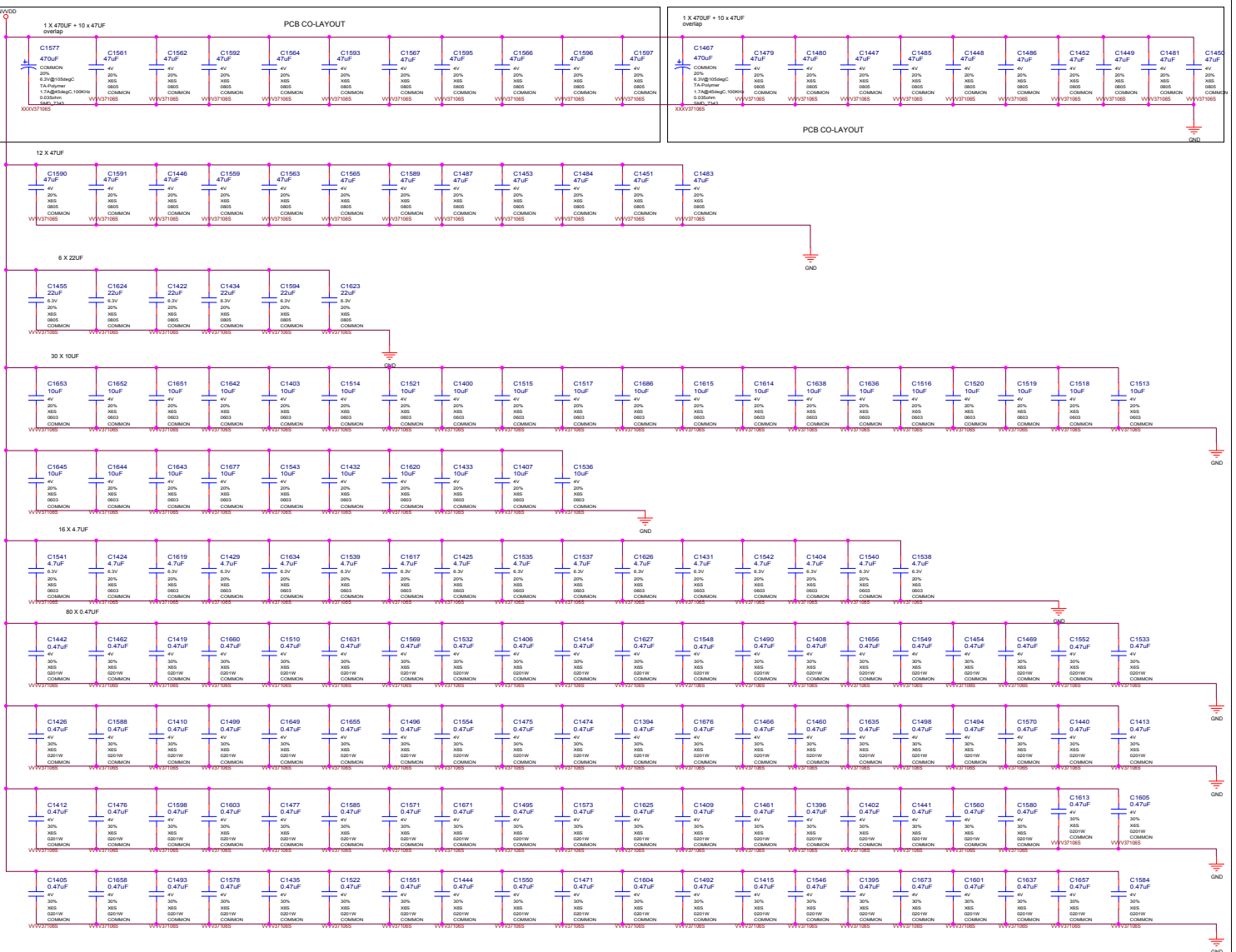
GPU PWR GND NCs



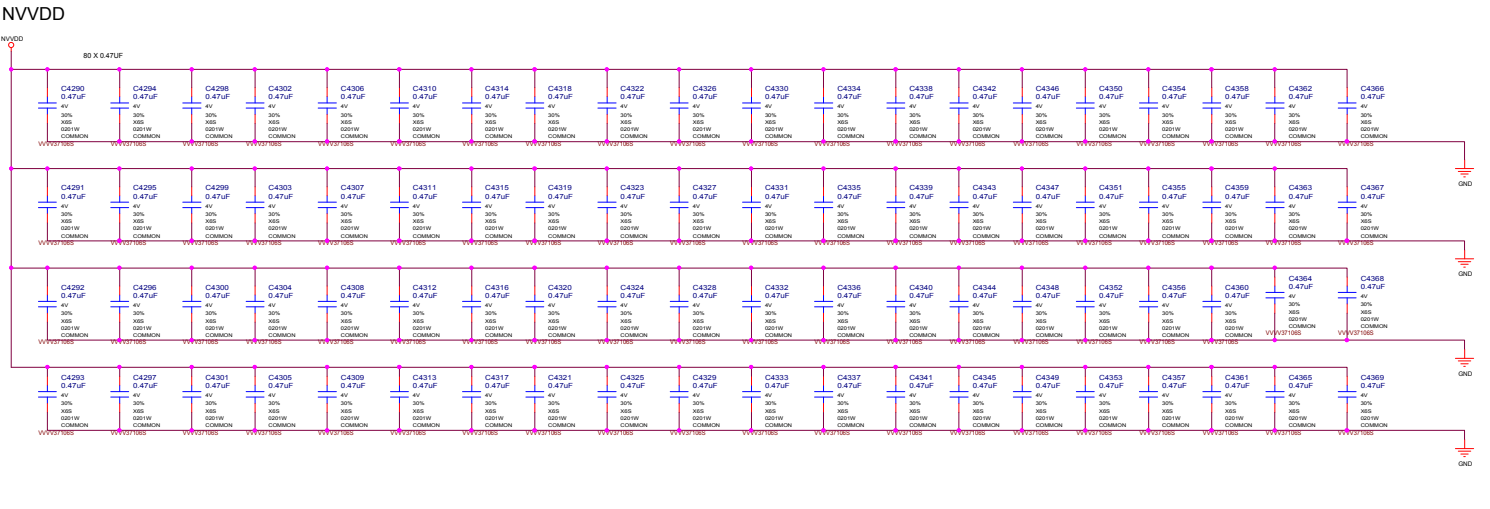
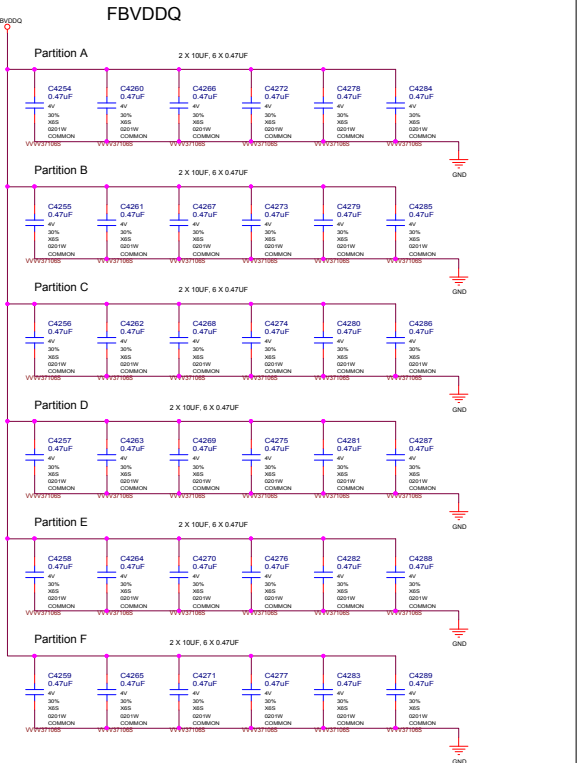
GPU Decoupling



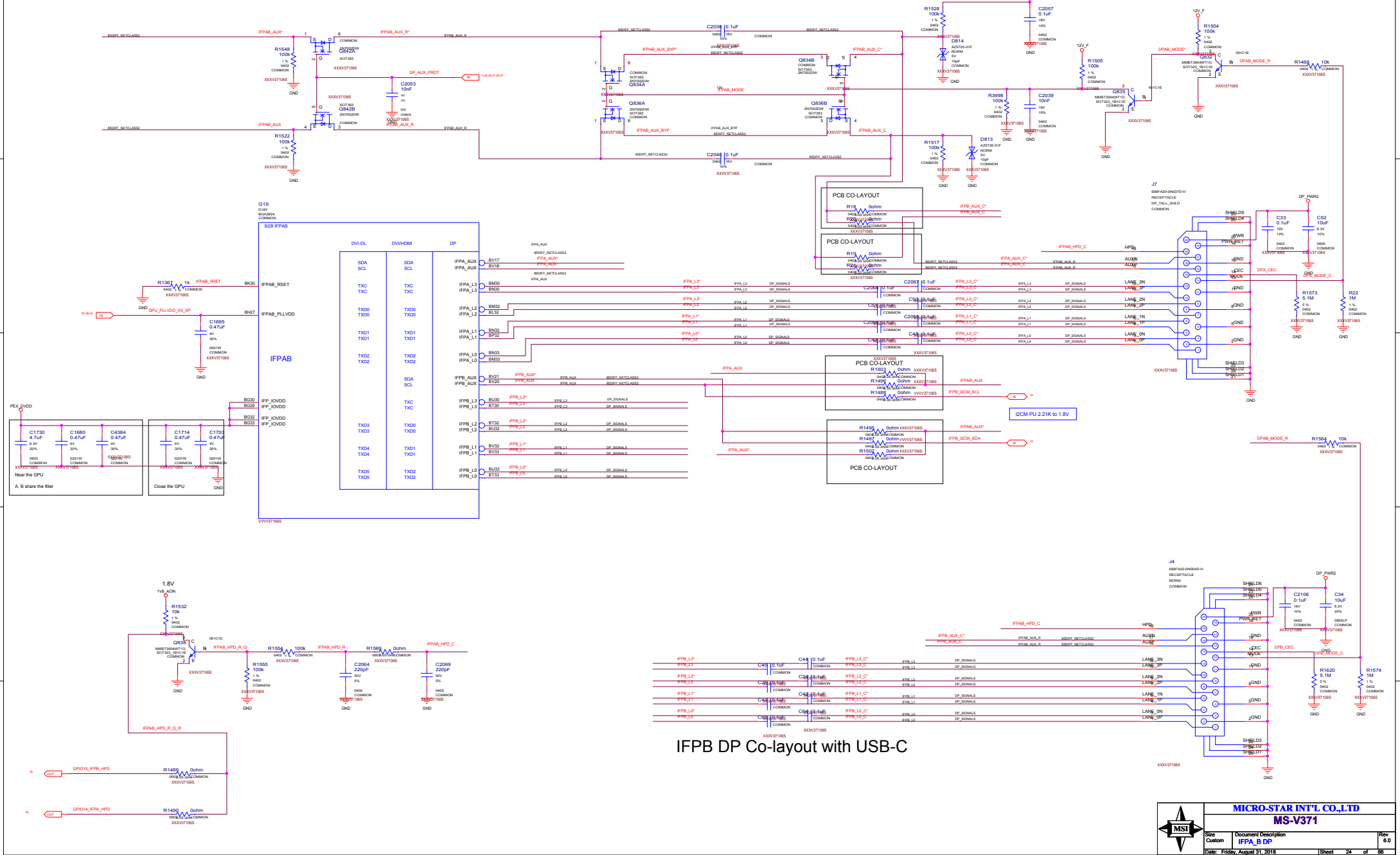
NVVDD



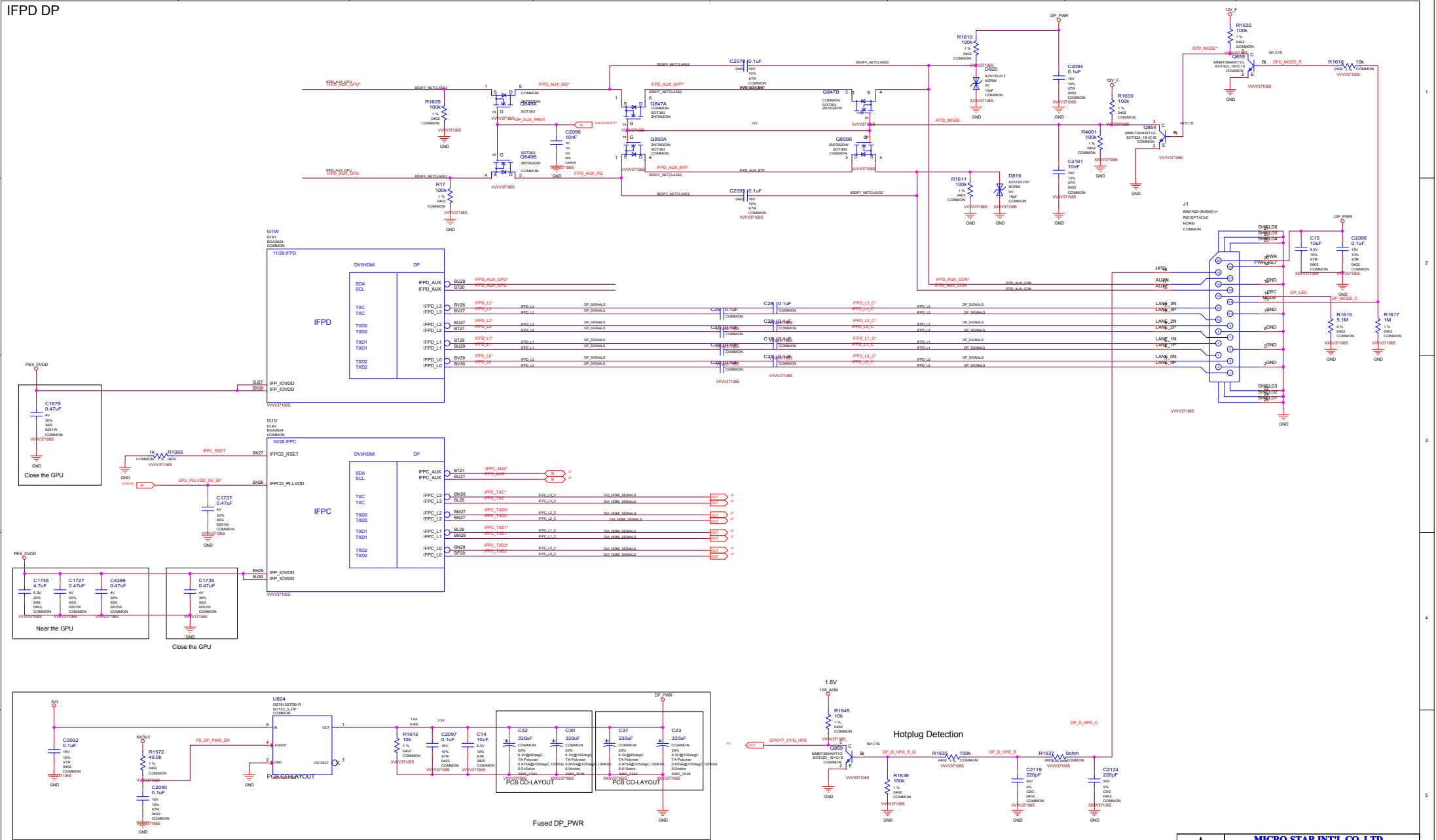
GPU Decoupling



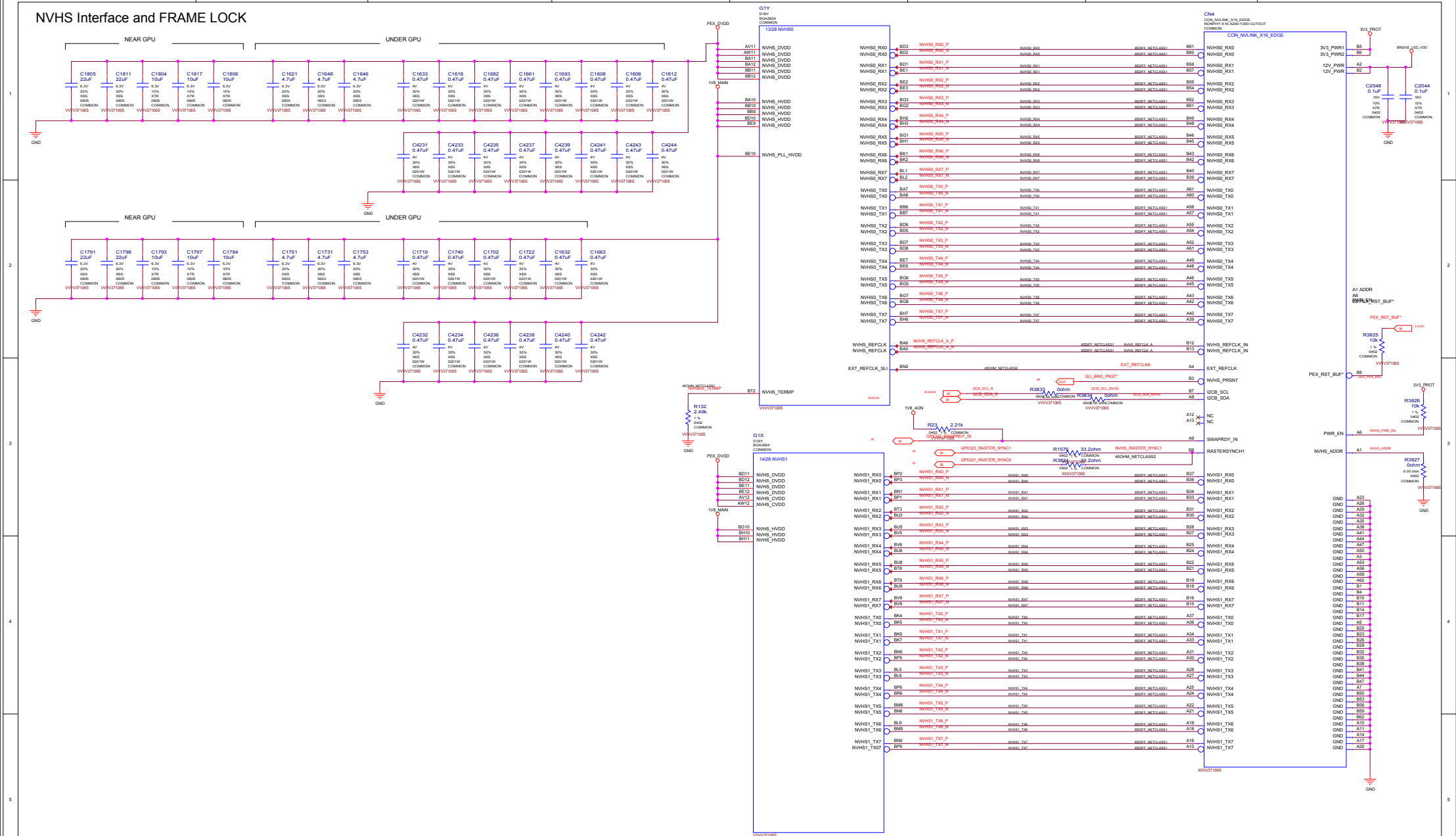
IFPAB TALL-DP



IFPB DP Co-layout with USB-C



NVHS Interface and FRAME LOCK



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MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00100
H	L	H	00101
H	H	L	00110
H	H	H	00111
L	L	M	01000
L	M	L	01001

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	H	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

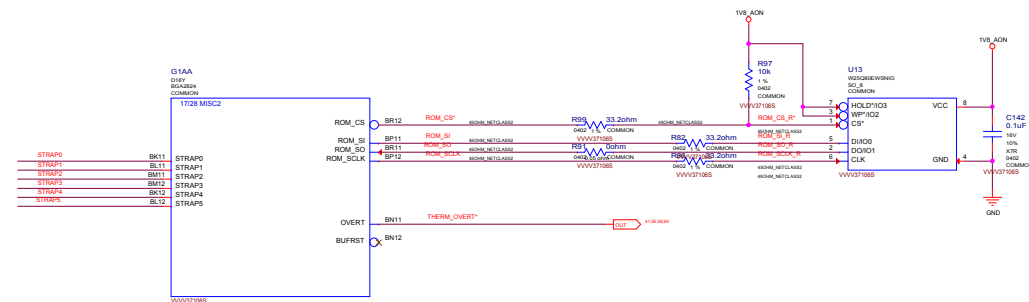
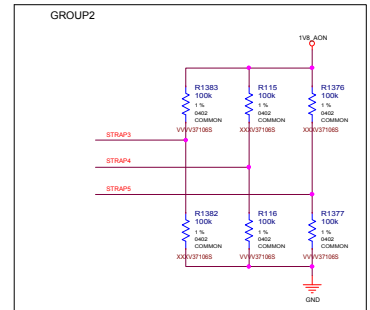
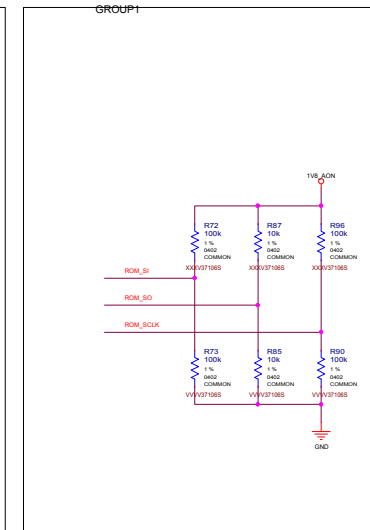
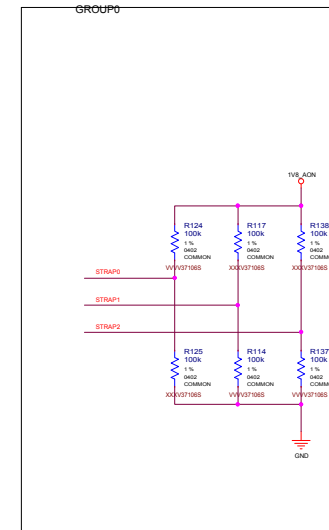
SKU 200

```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

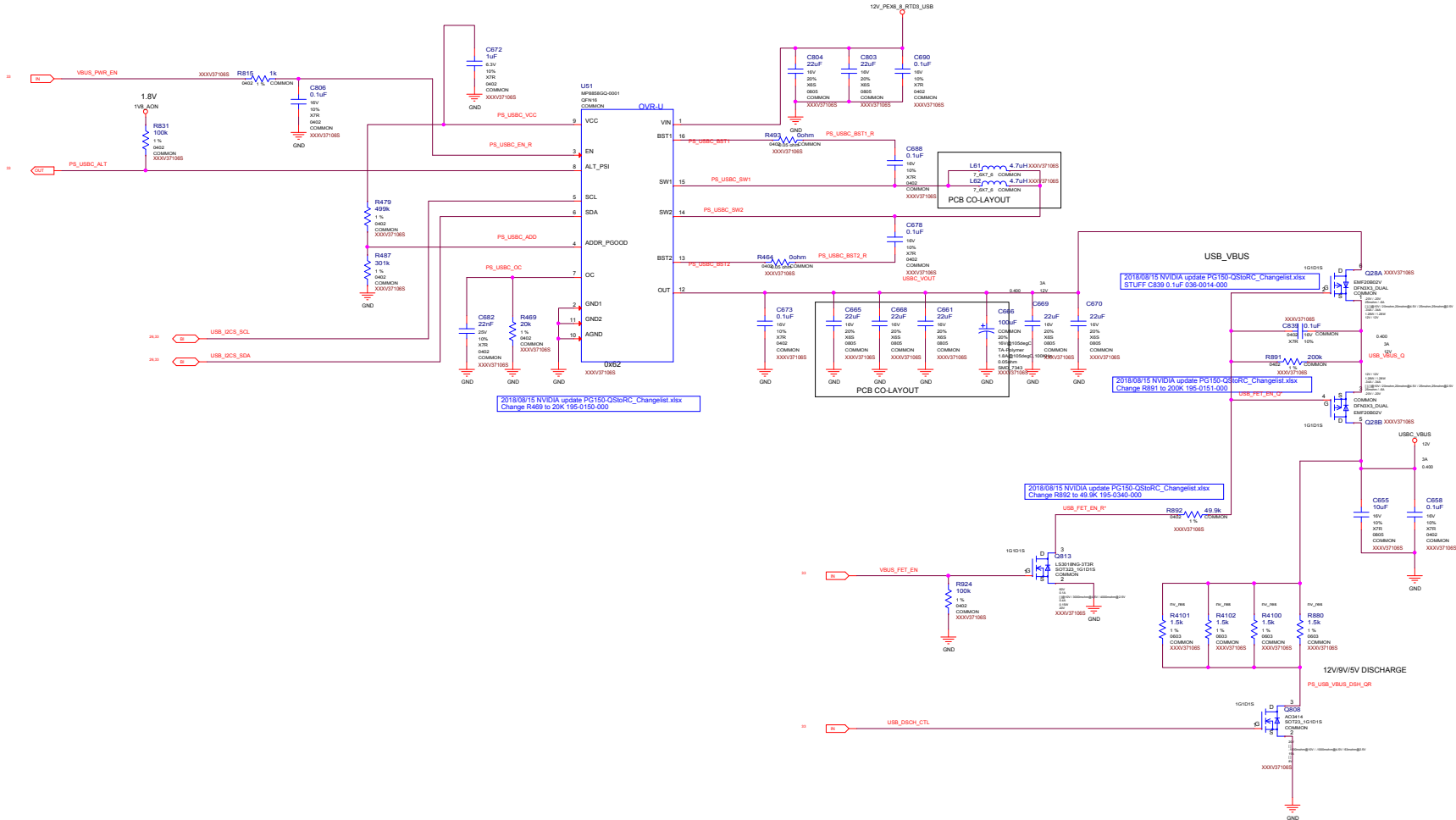
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
```

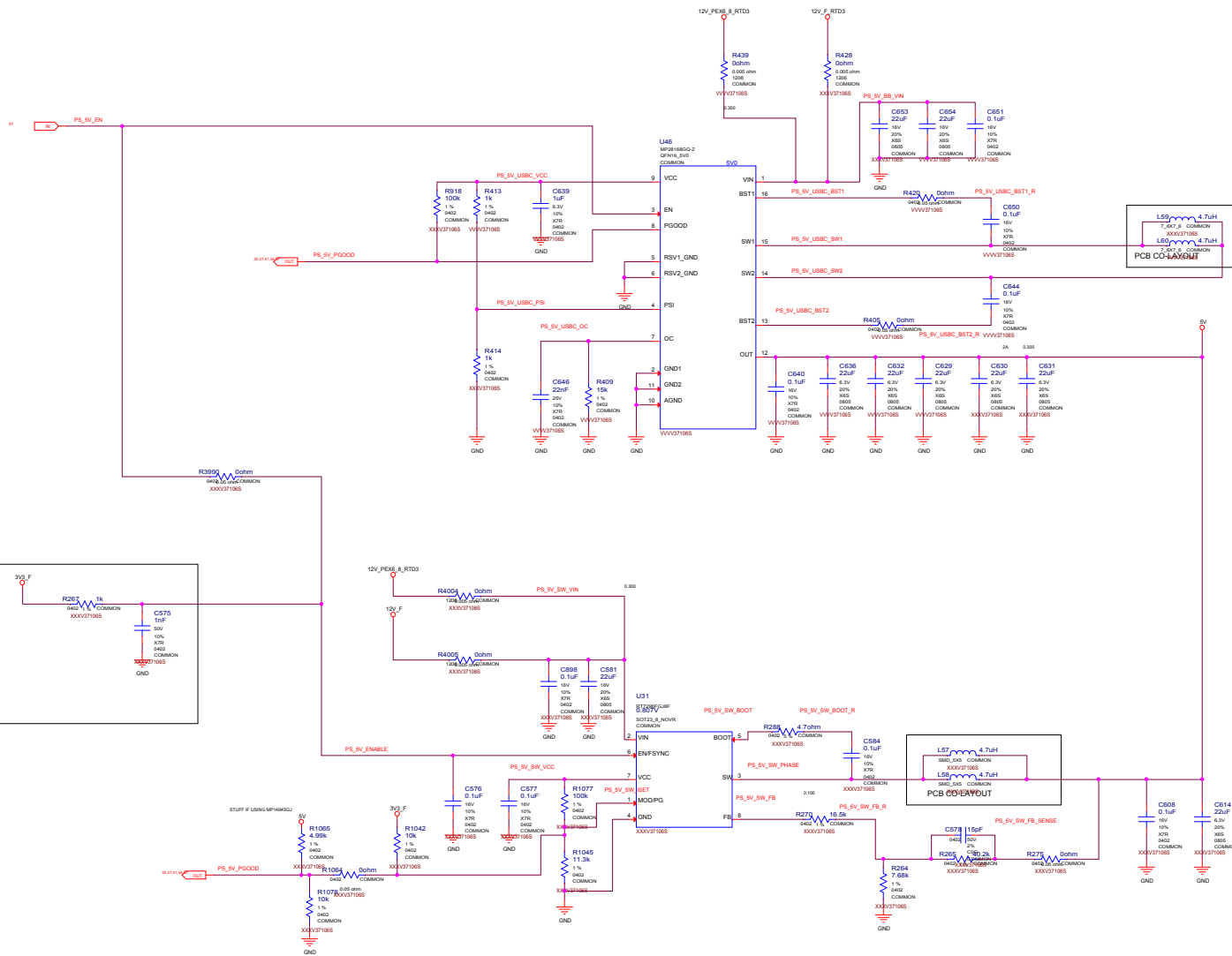


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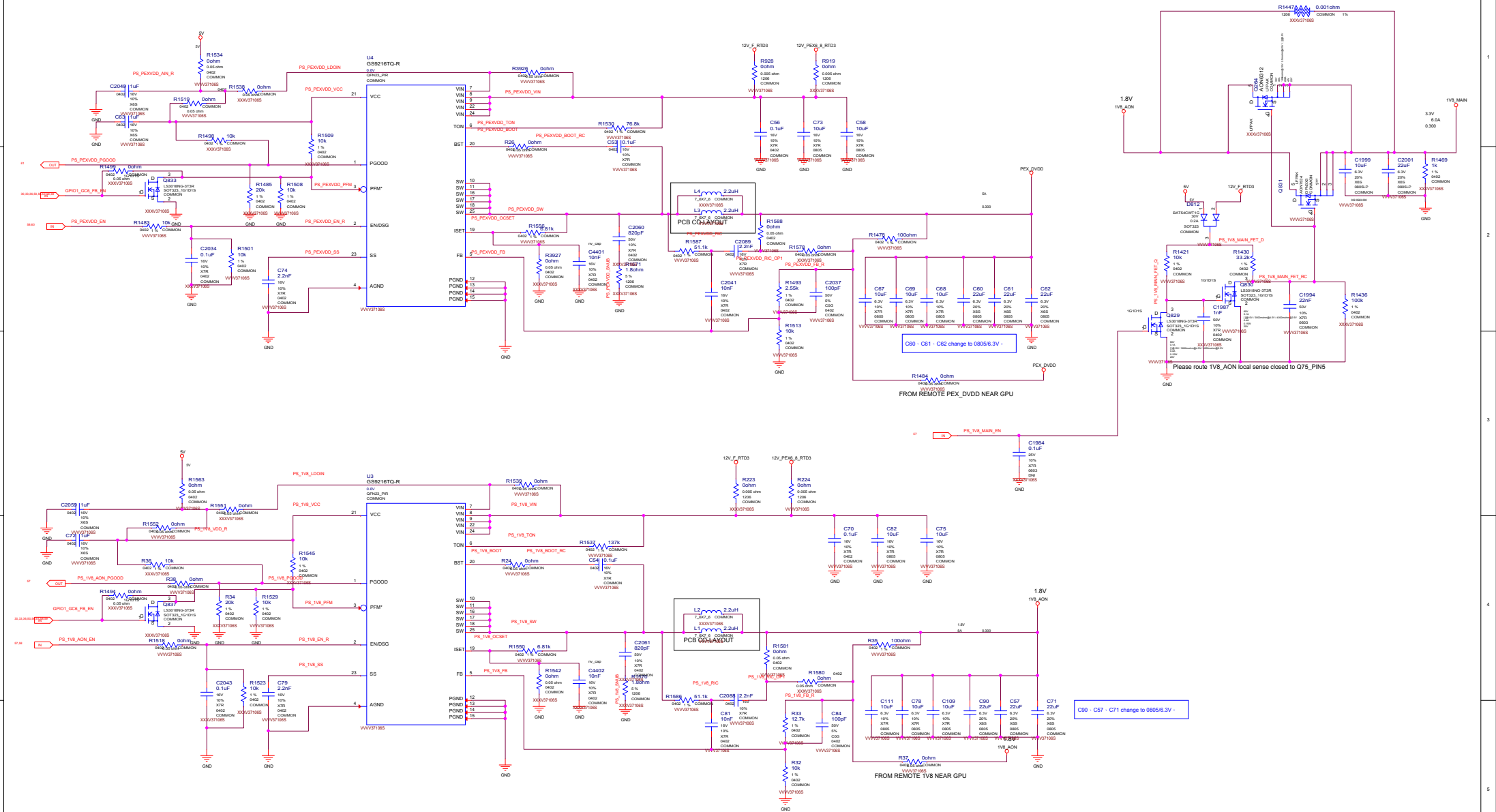
Size Custom	Document Description ROM/STRAPS	Rev 6.0
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PS: 5V, 5V_BACKUP



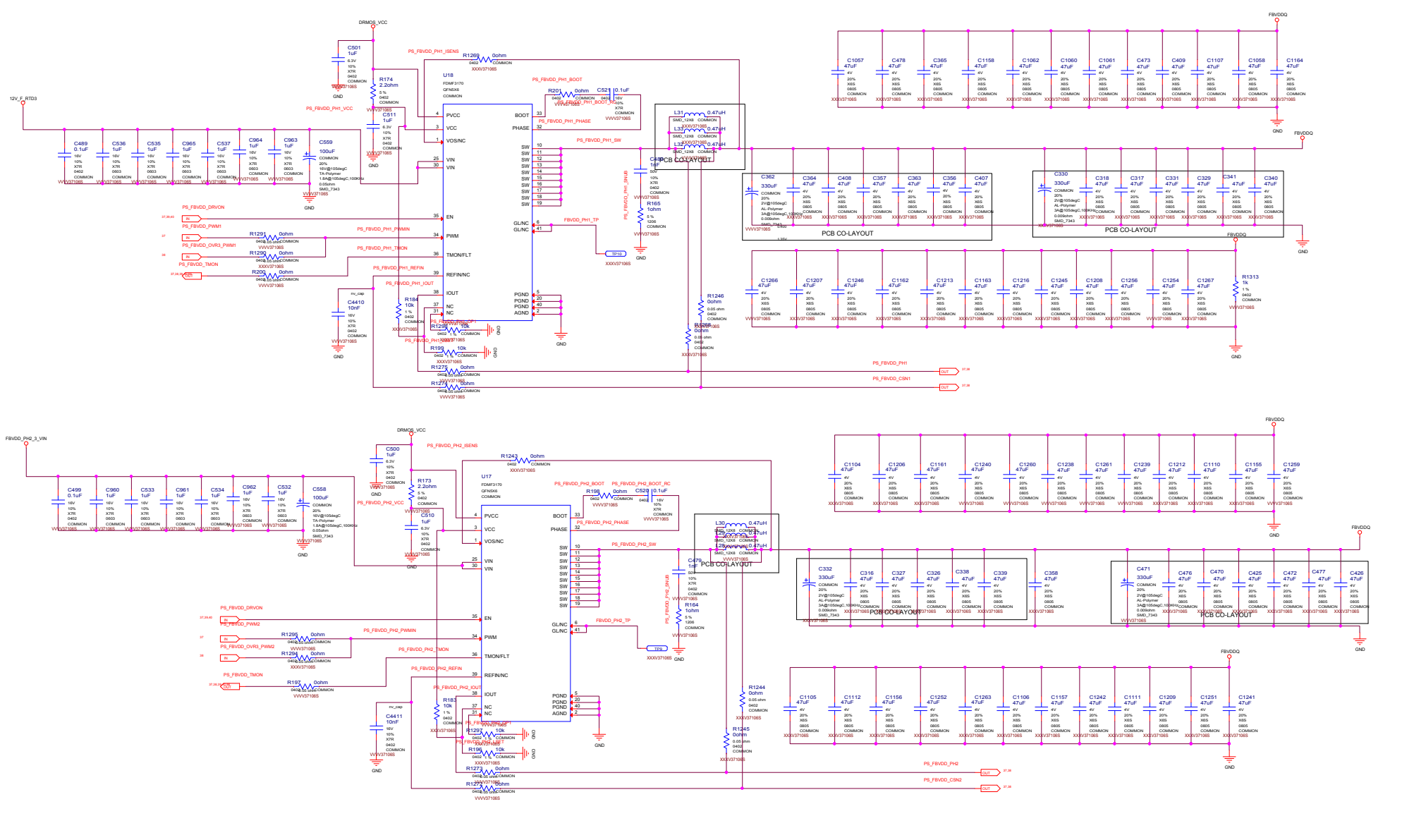
PS: PEXVDD 1V8 Rail



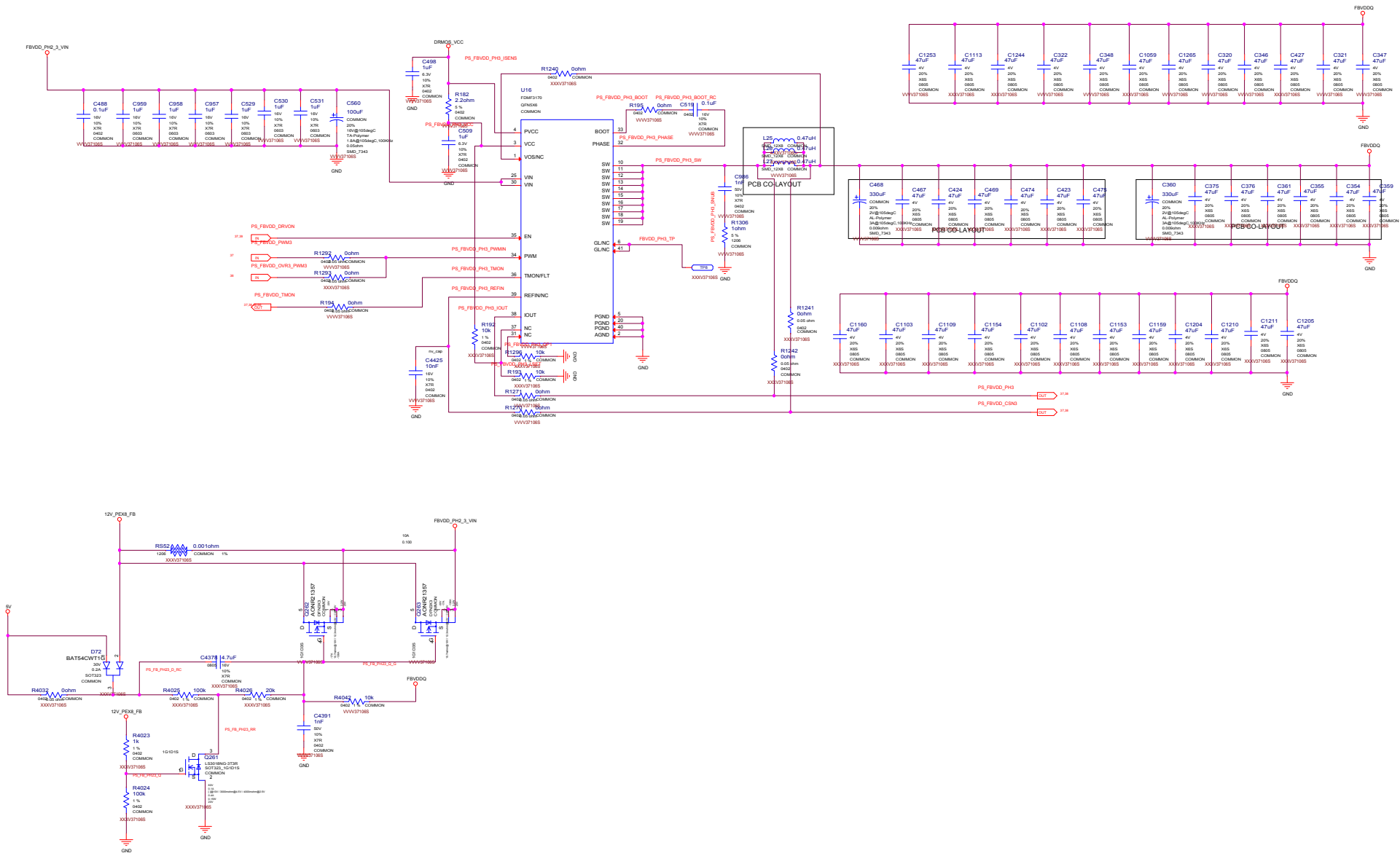
MICRO-STAR INT'L CO.,LTD
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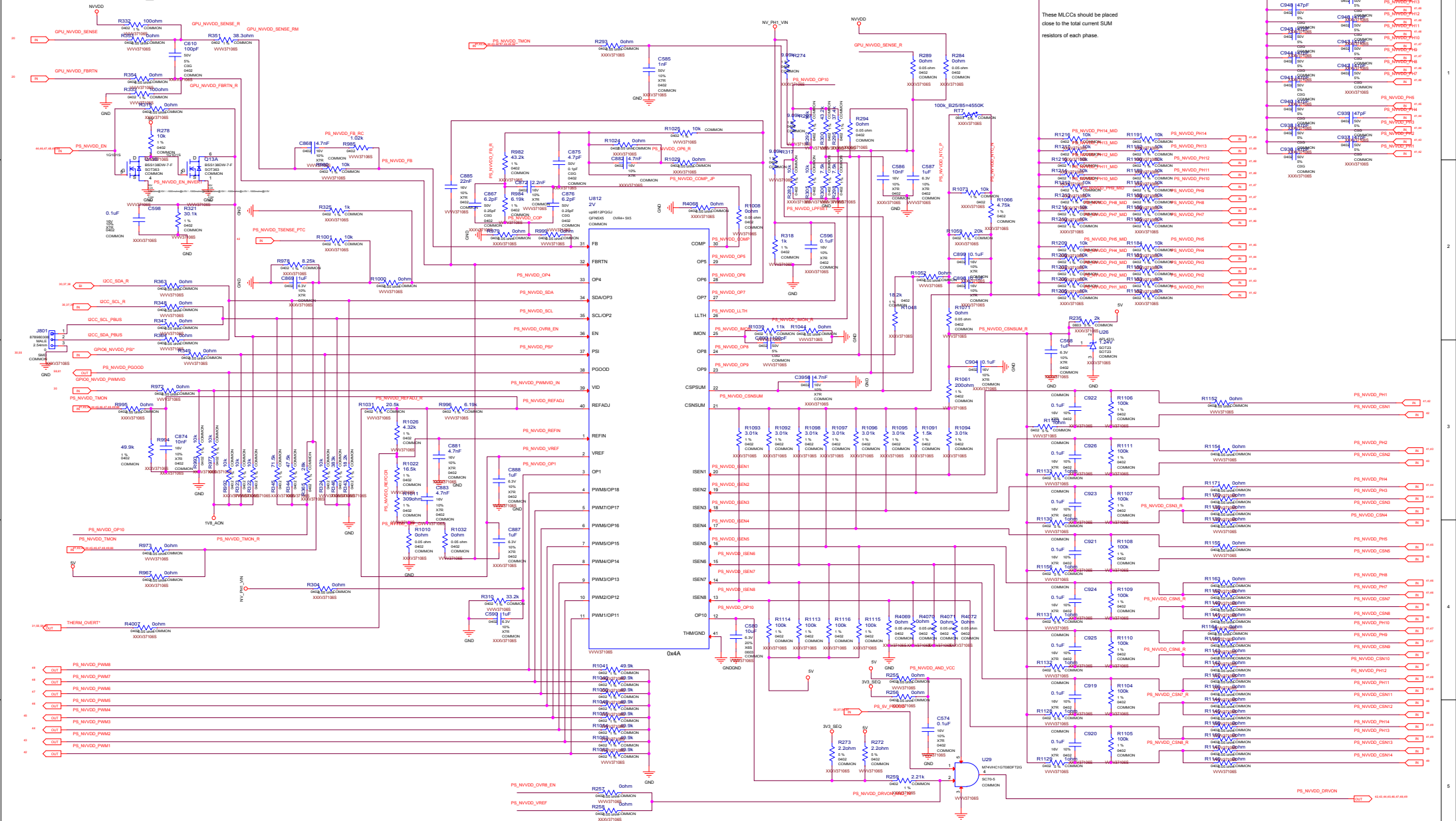
PS: FBVDD PH1, 2



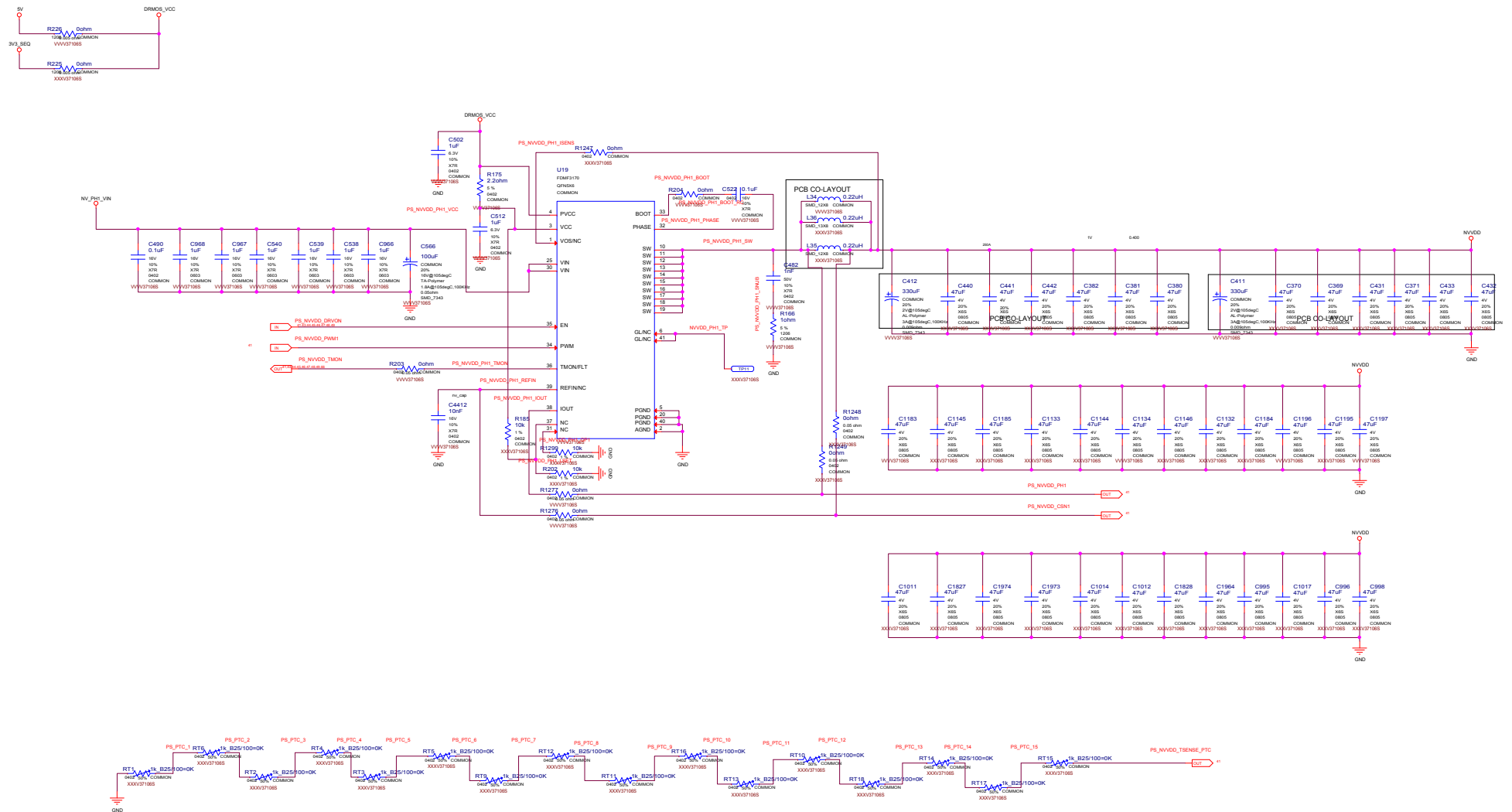
PS: FBVDD PH3

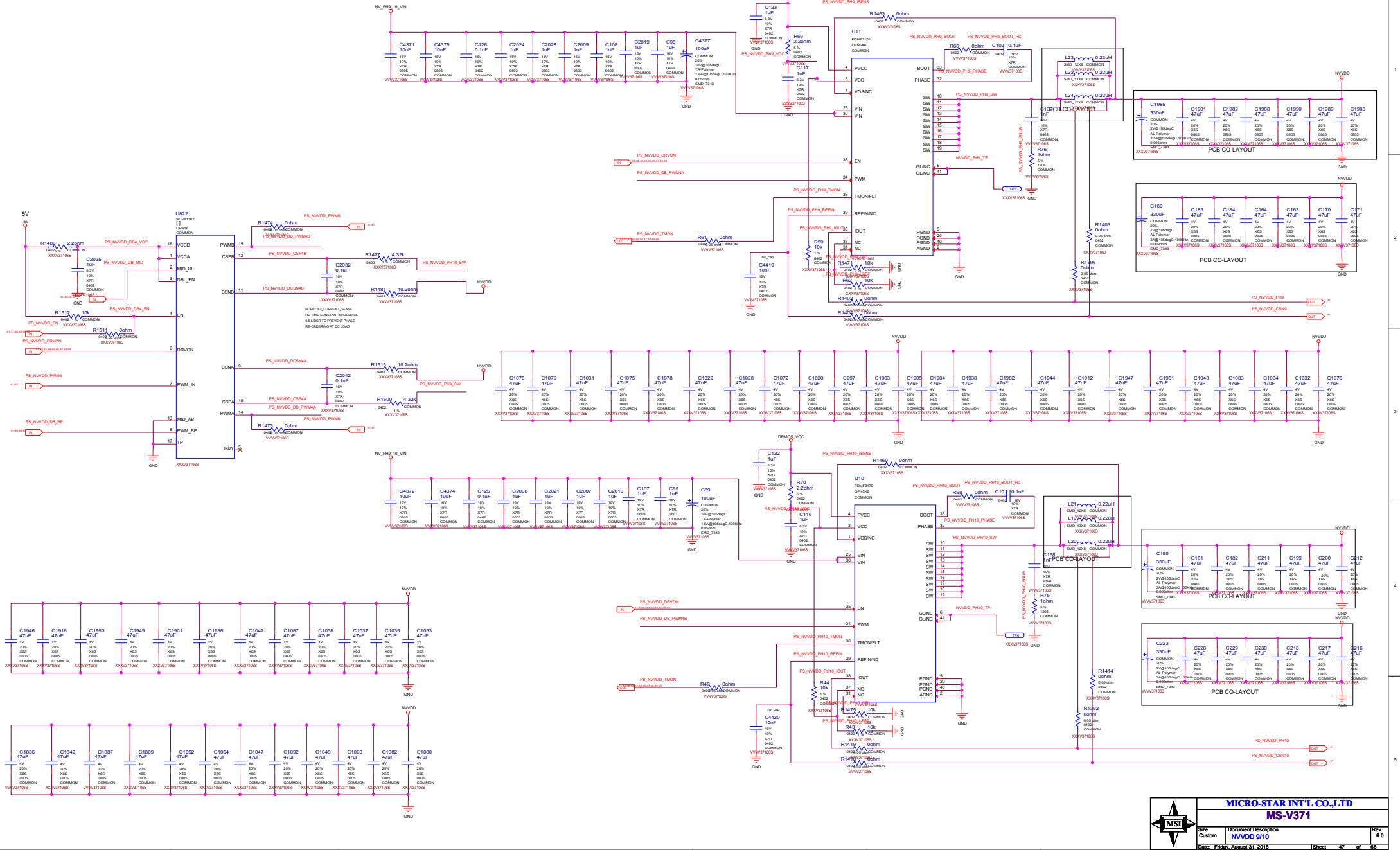


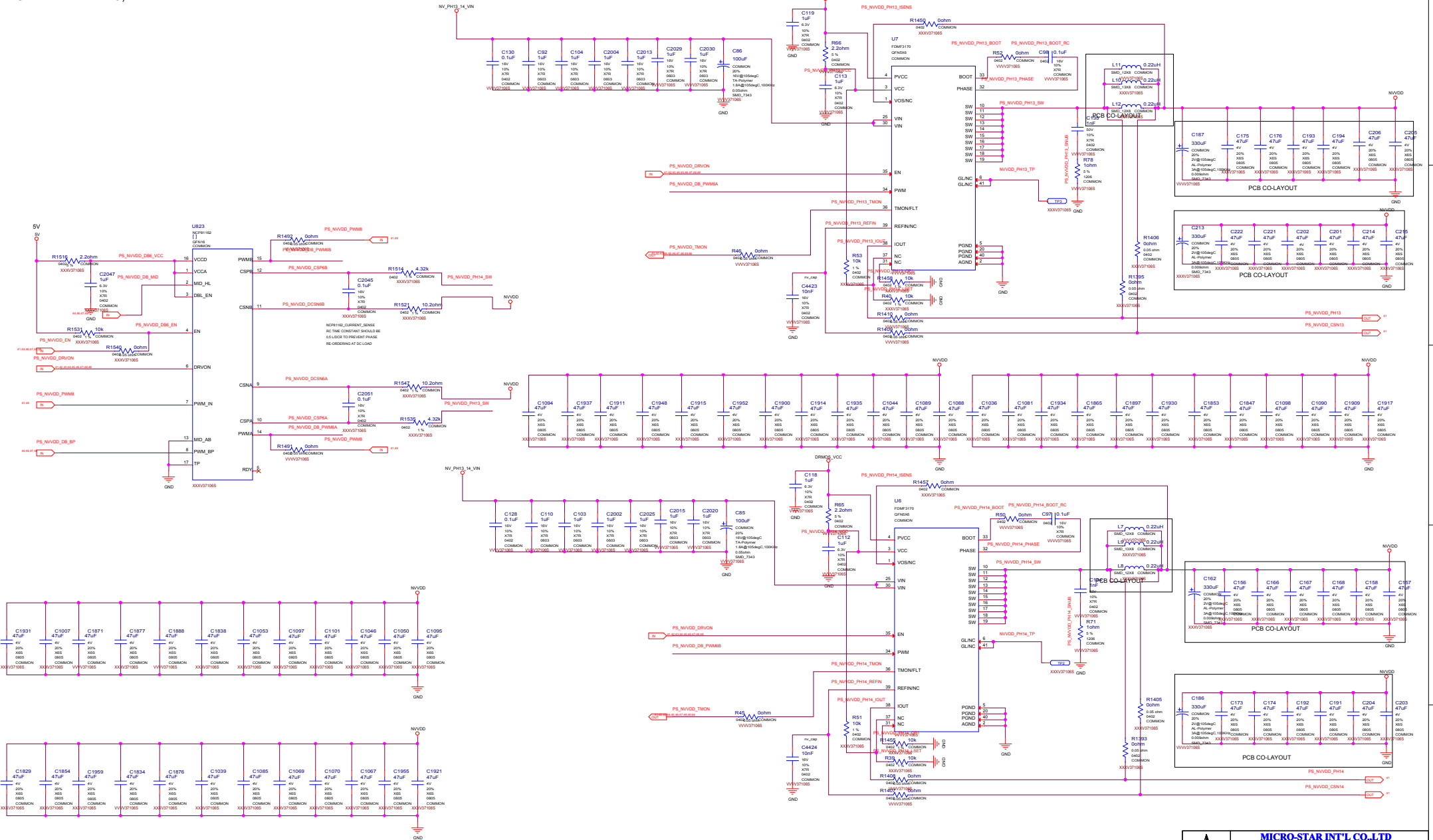
PS: NVVDD Controller_OVR8



PS: NVVDD Phase 1







PS: INPUT SWITCH RTD3

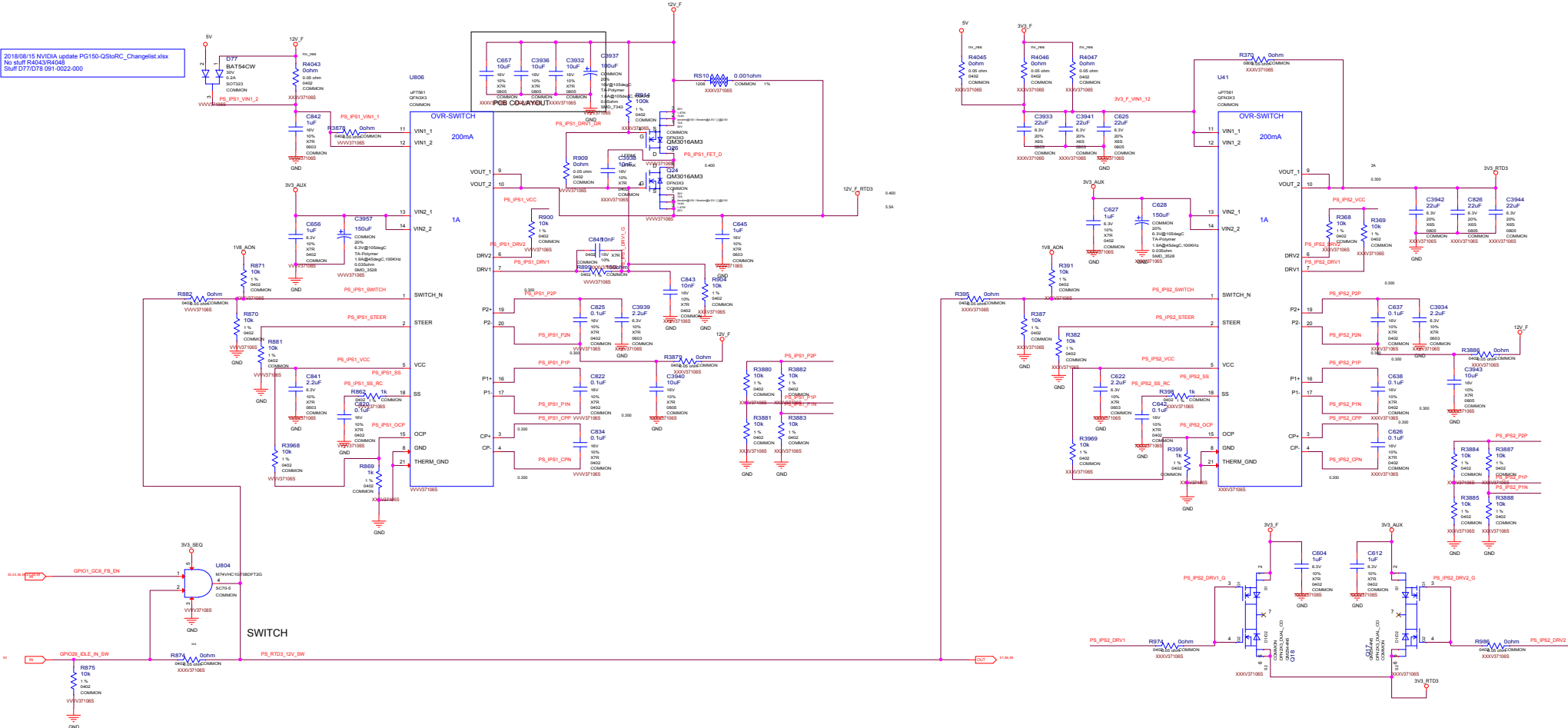
AND GATE LOGIC FOR P-BOARD

GPI01	GPI029	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

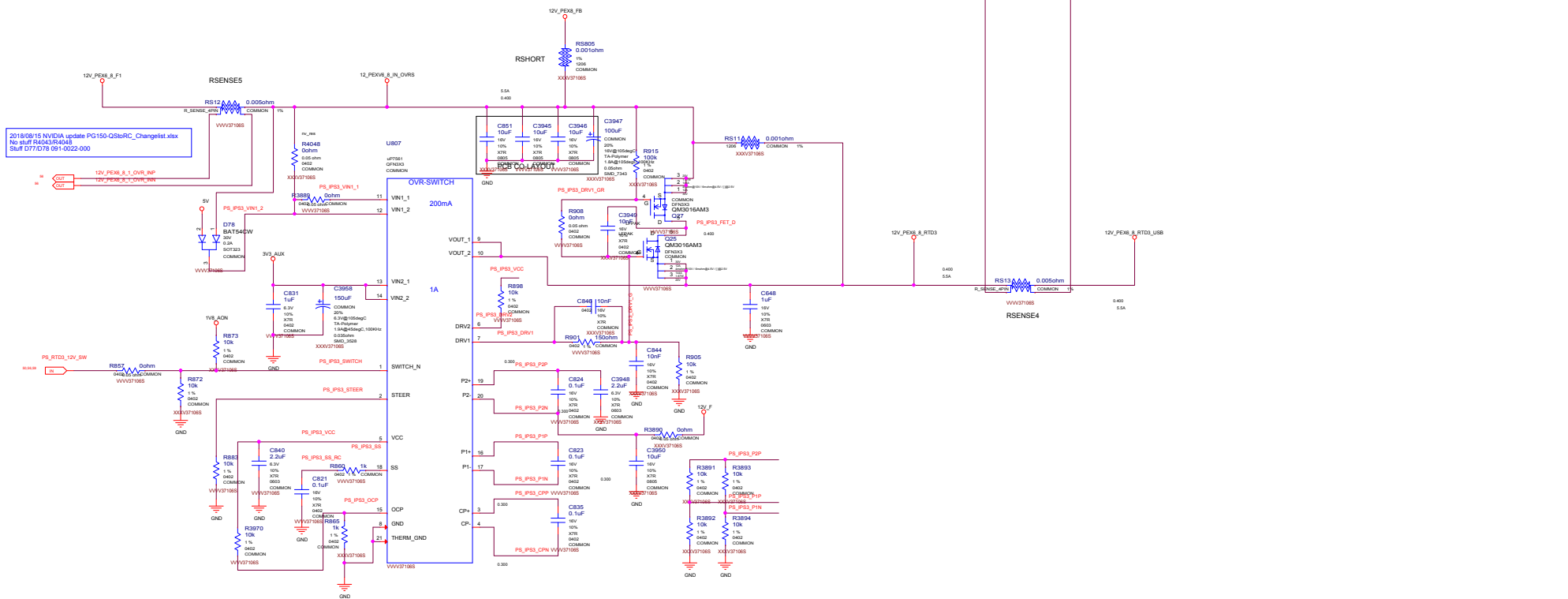
AND GATE LOGIC FOR P-BOARD

GPI01	GPI029	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

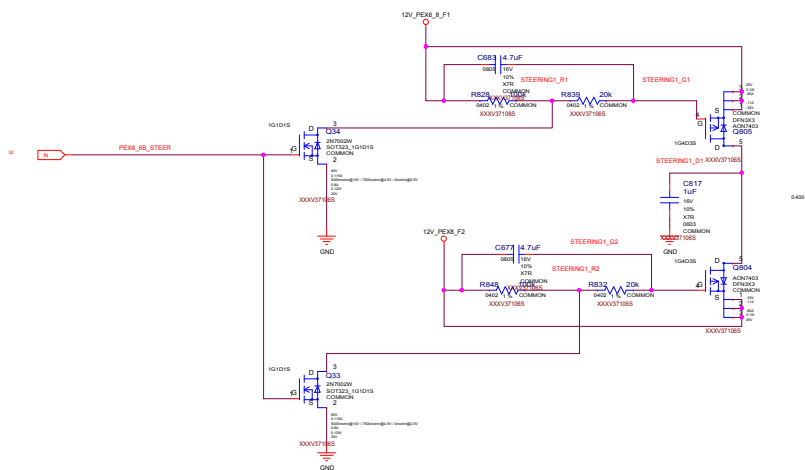
2018/08/15 NVIDIA update PG150-QStoRC_Changelist.xlsx
No stuff R4043/R4048
Stuff D71078 091-0022-000



delete INA3221

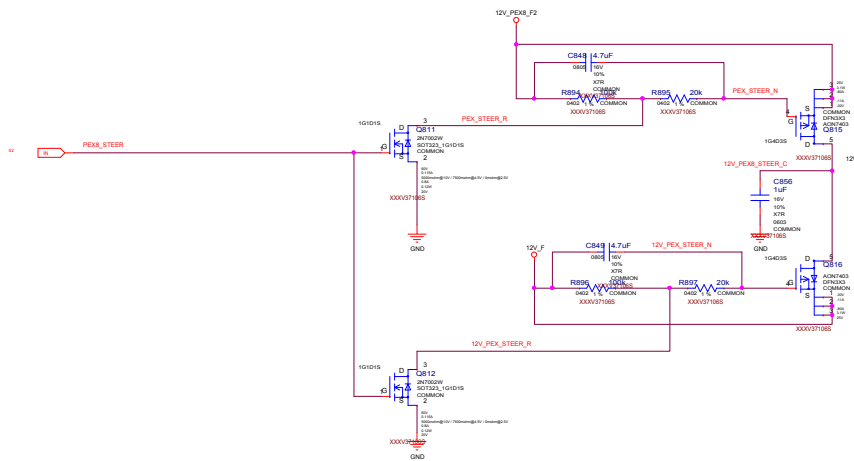


12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

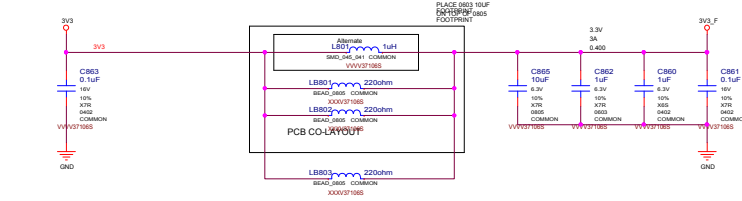
For OpenVing Type4 + Phase Doubler, 2 phase PSI mode



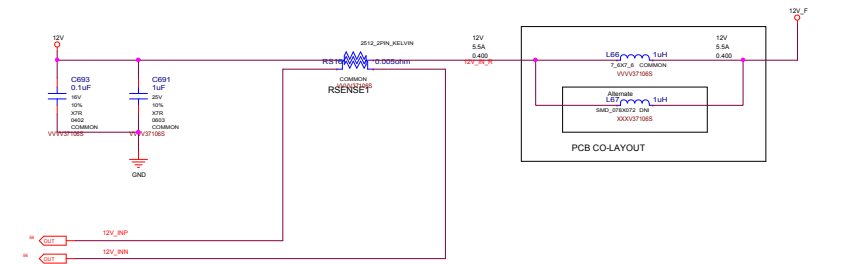
PS: Inputs, Filtering, and Monitoring

delete INA3221

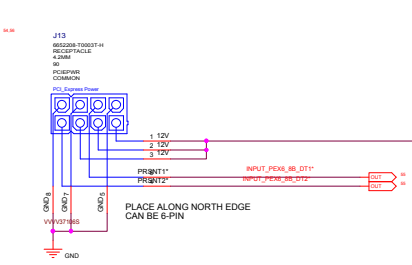
PEX 3V3 INPUT - 10W



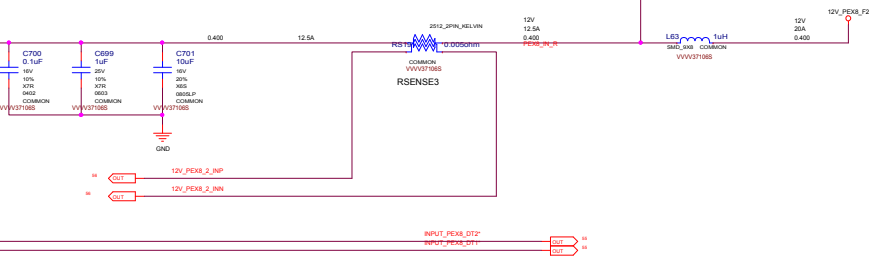
PEX_12V INPUT - 66W



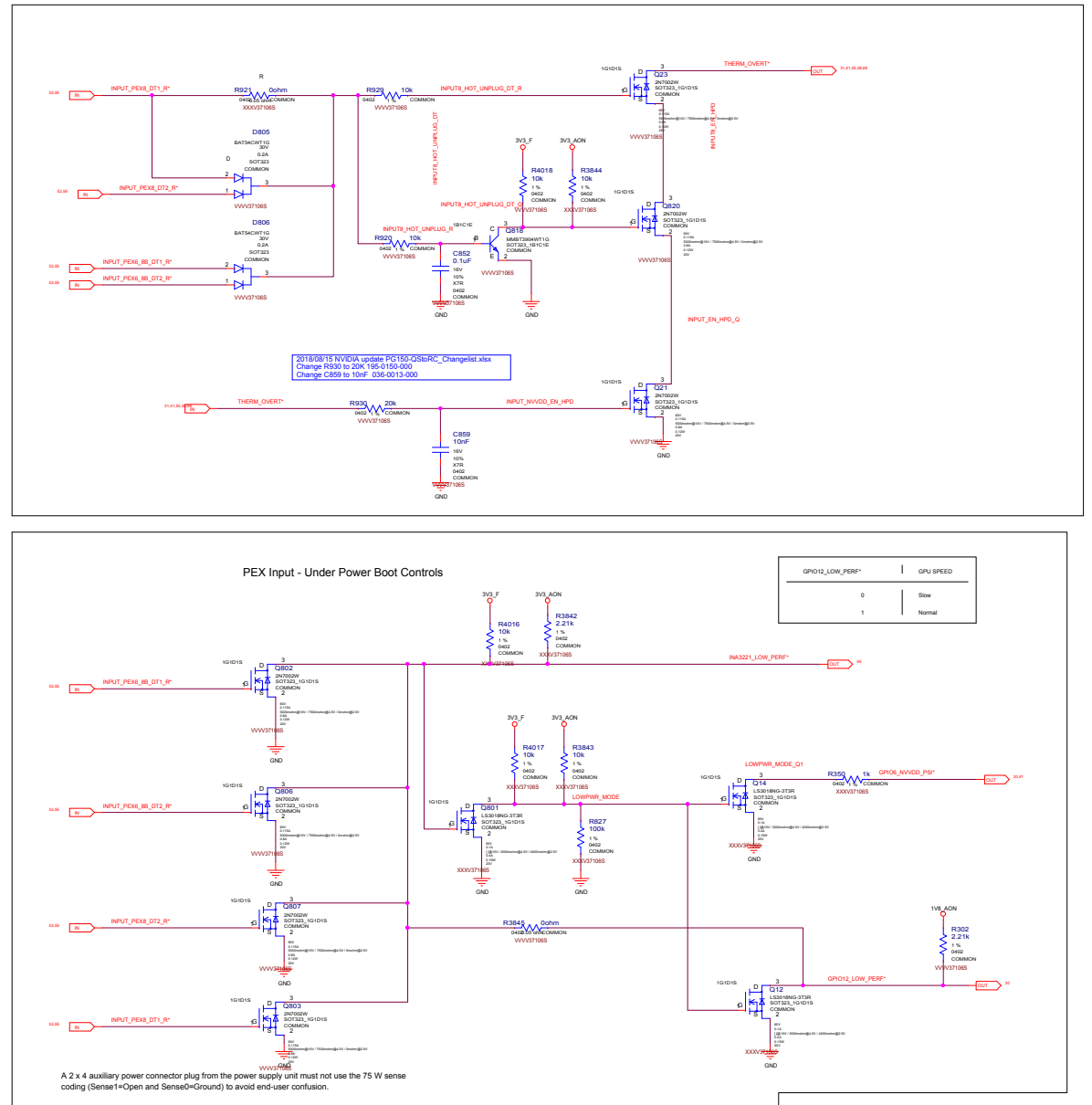
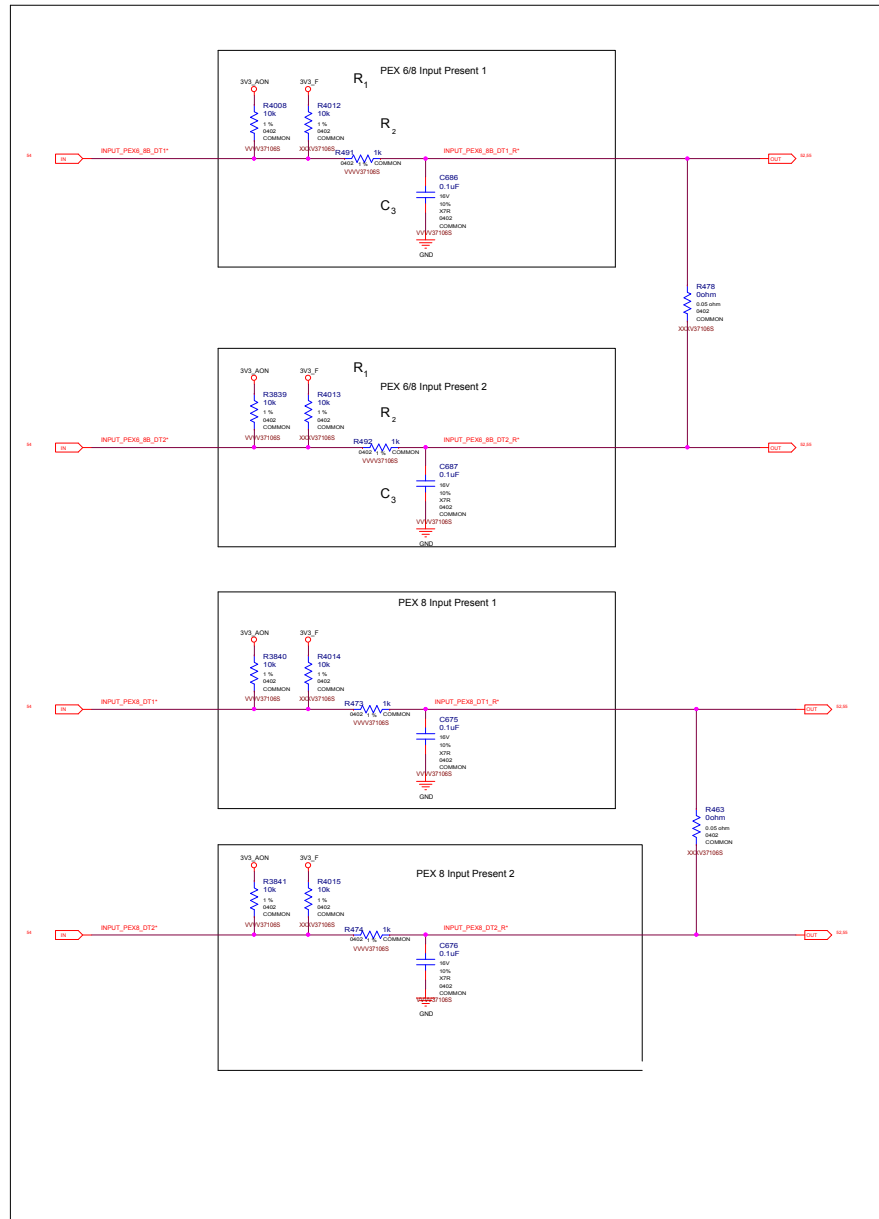
PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W

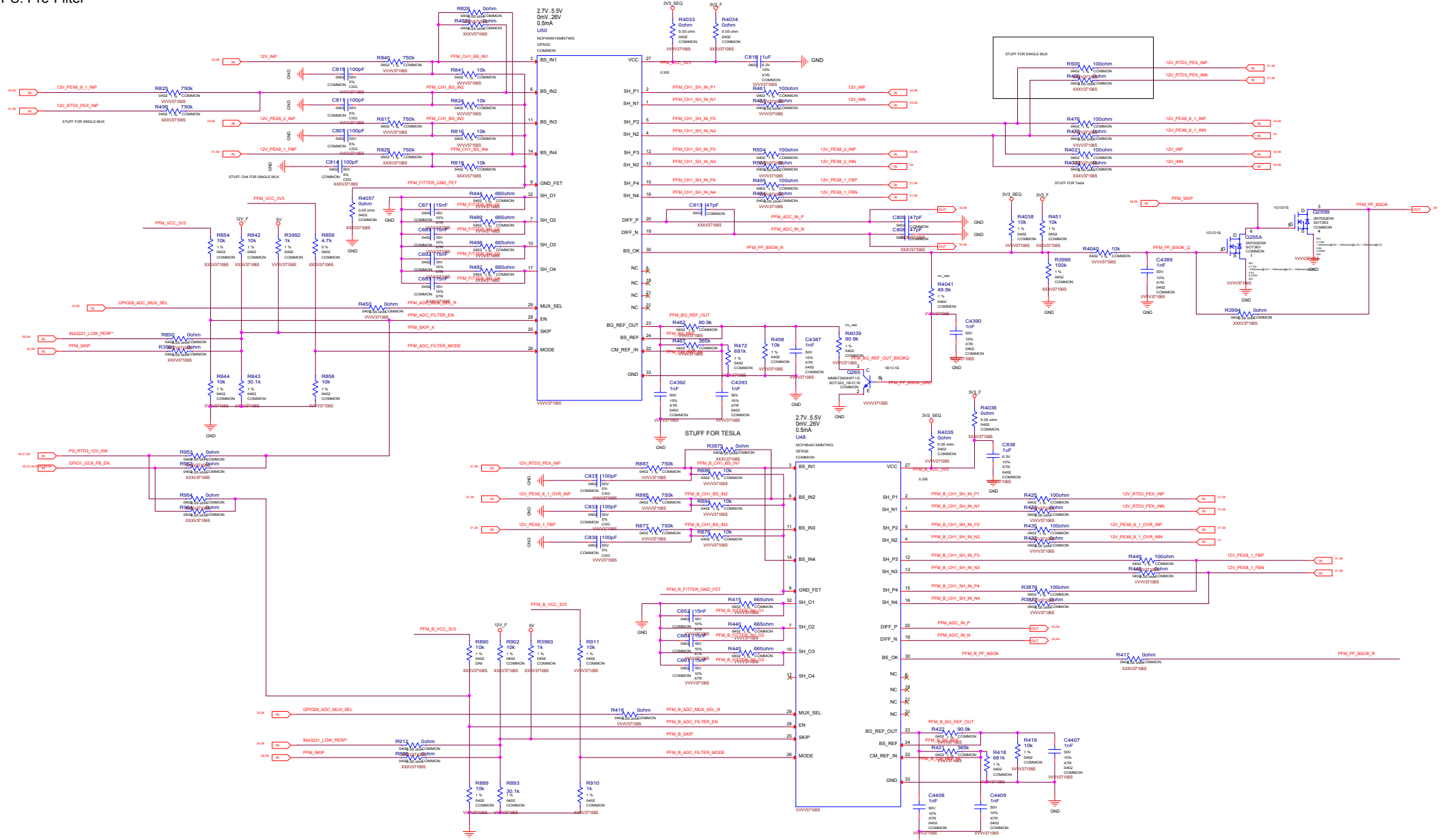


PS: 12V Current Steering & Hot Unplug Detect

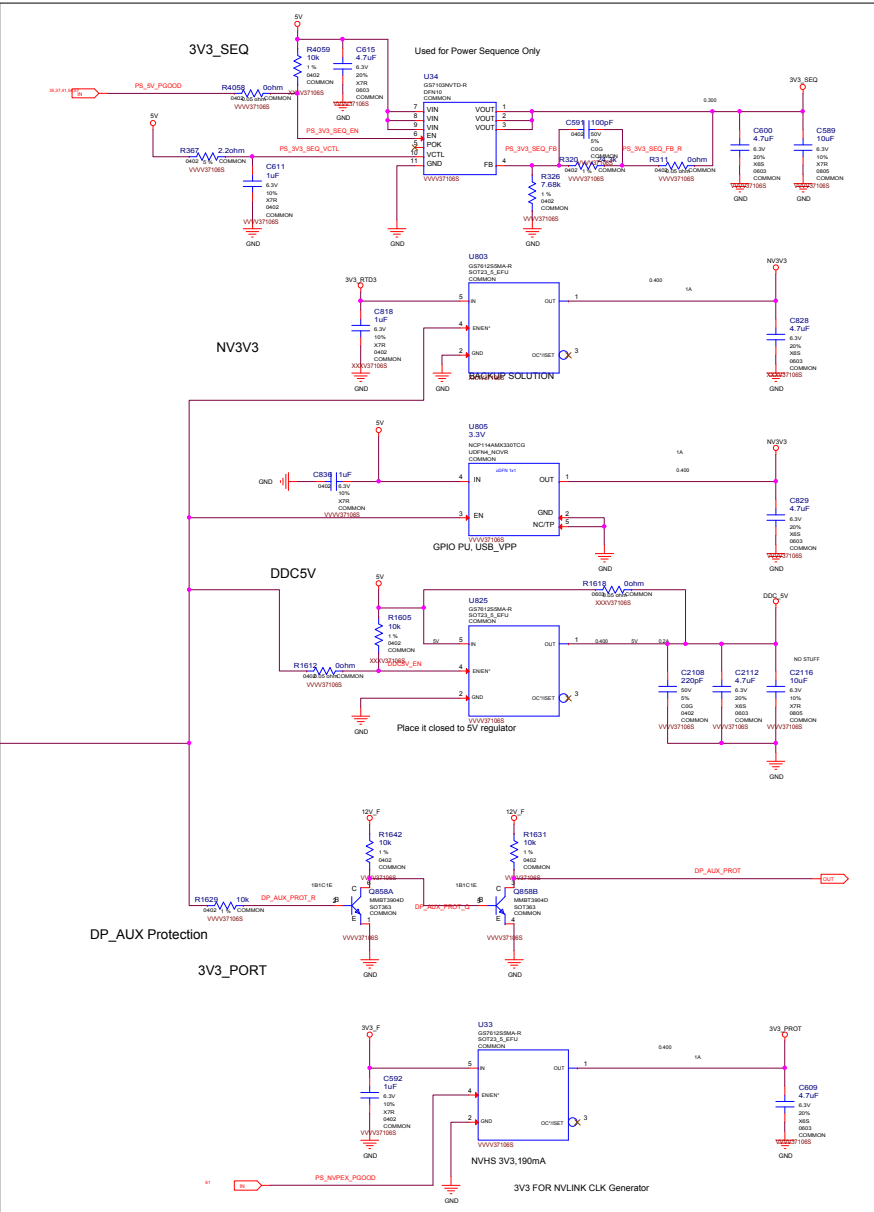
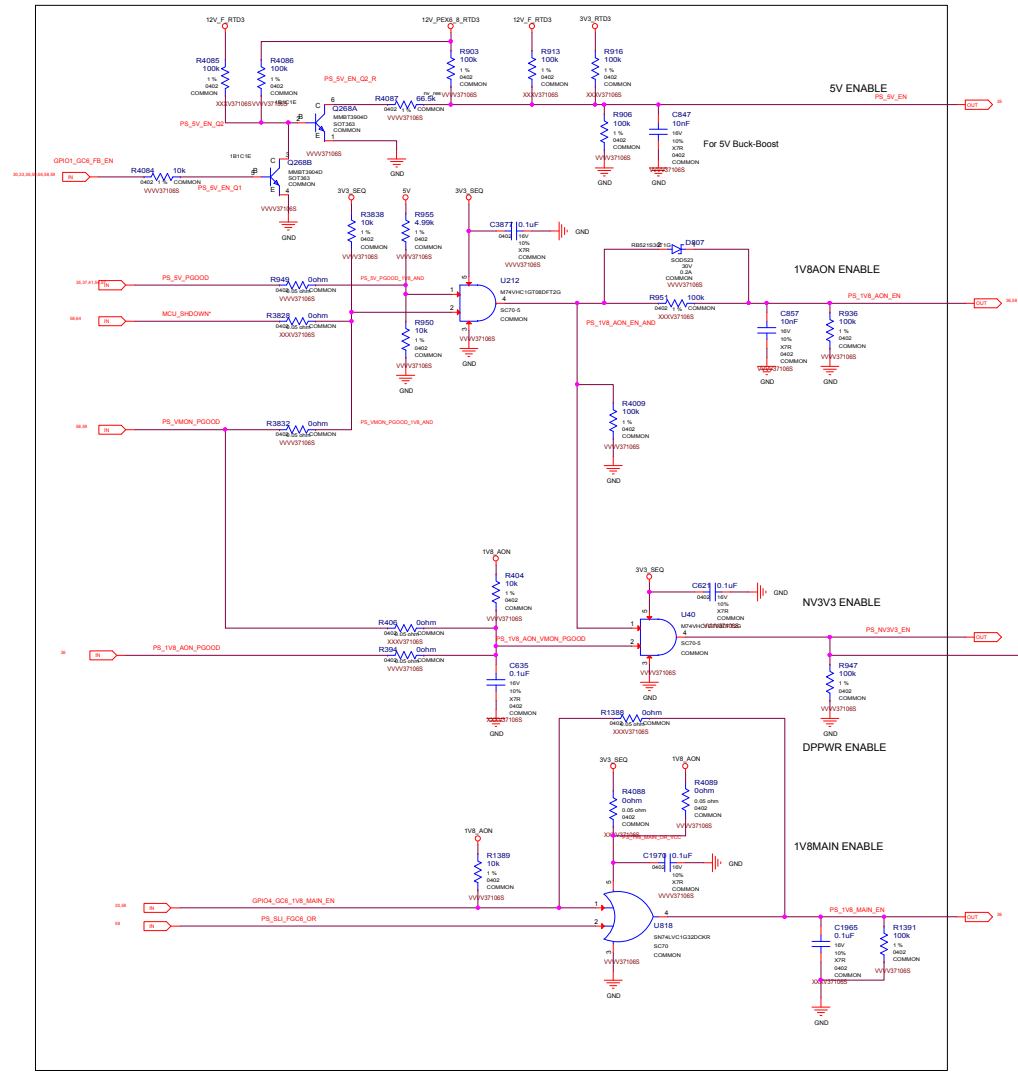


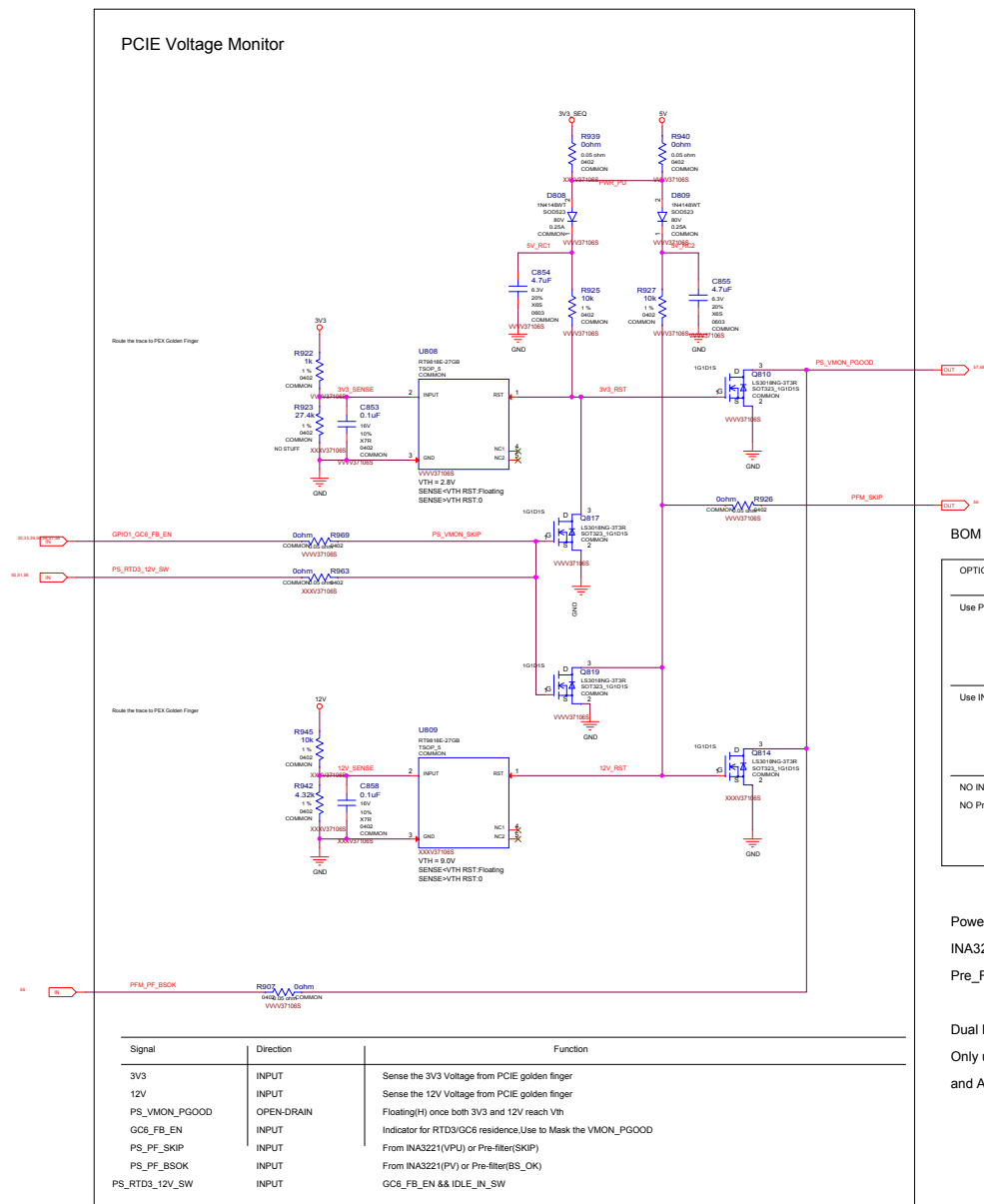
PS: Pre-Filter

STUFF IF USING 2XMUX



SEQUENCE:5V,1V8,NV3V3 ENABLE





BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

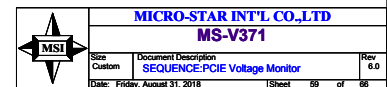
INA3221:3V3_SEQ

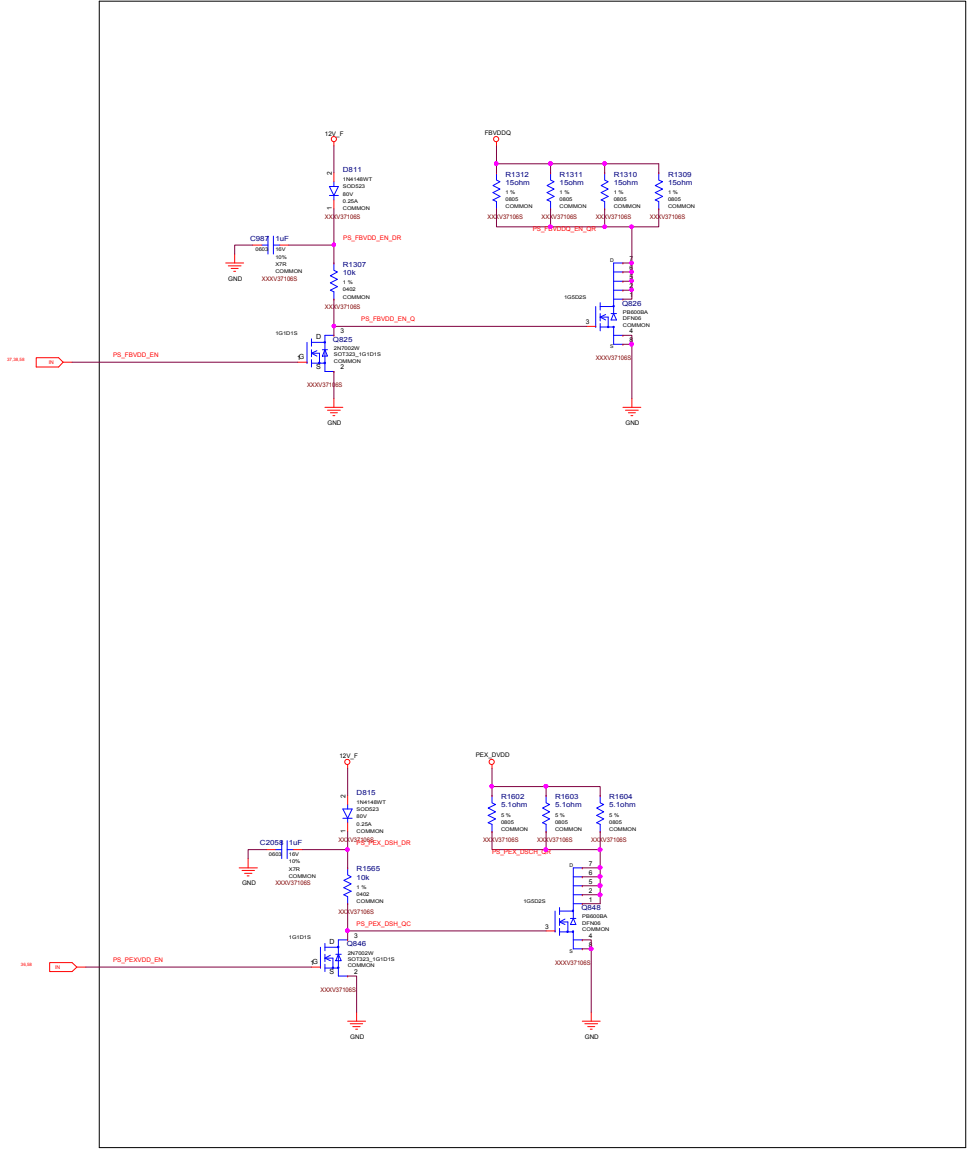
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

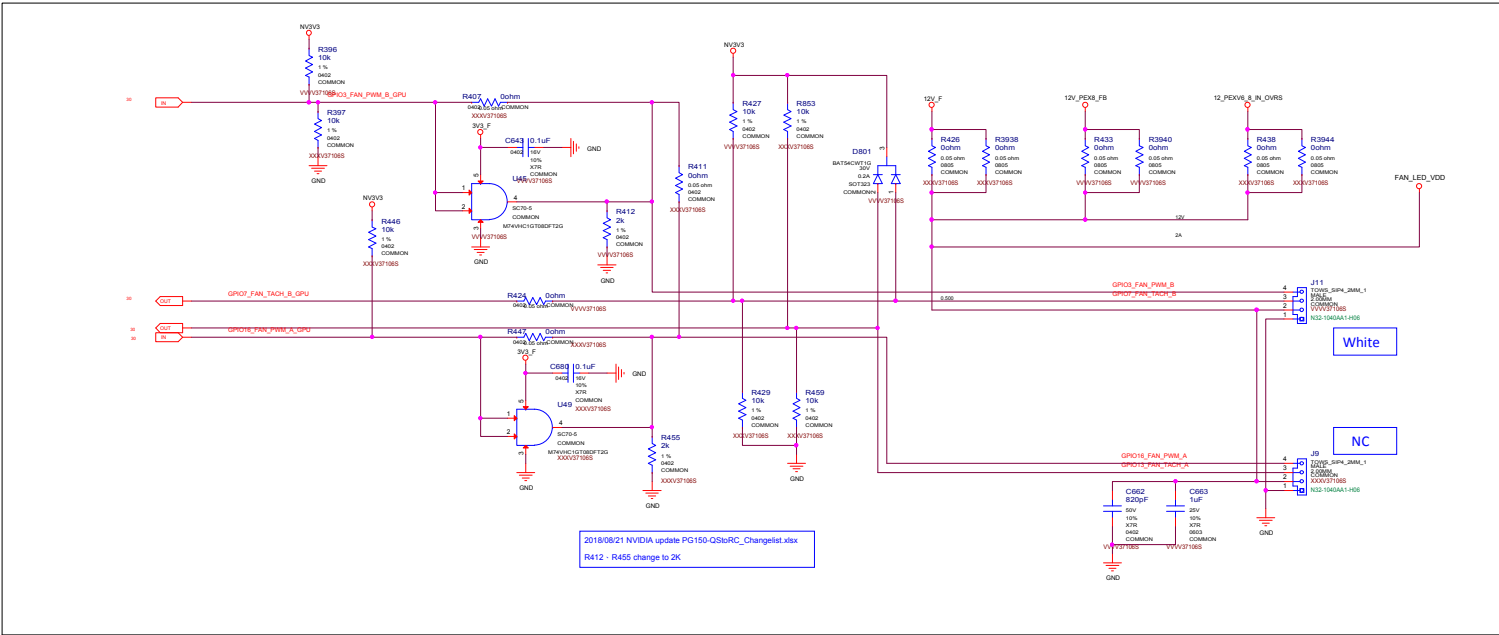
and All Input 12Vs





MISC: FAN & LED1

delete RGB control signals



LED BOOST

delete LED's power

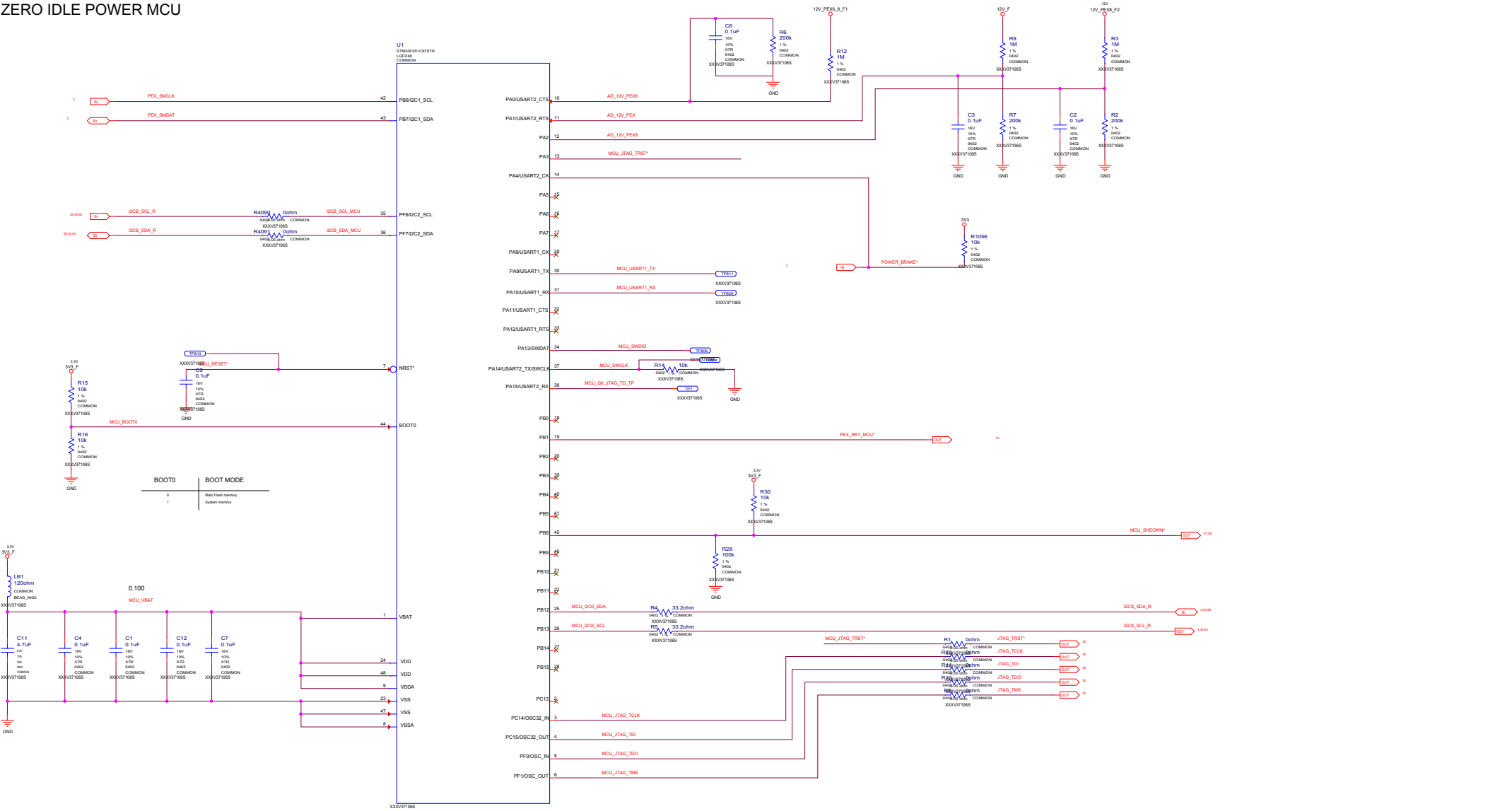


MISC: LED2



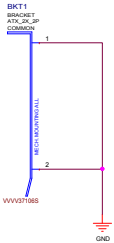
delete RGB control signals

ZERO IDLE POWER MCU



Mechanical: Bracket/Thermal Solution

Brackets:



Bracket Screw



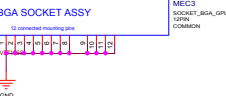
Back Cover



GPU Stiffener back side



GPU Socket Symbol



Bracket Screw

BKTSREW1



BKTSREW2



FAN1



HDMISREW1



HDMISREW2



HS1



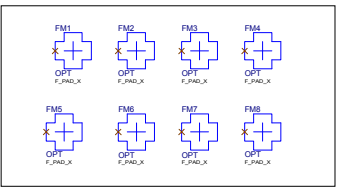
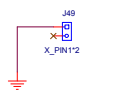
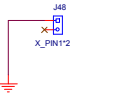
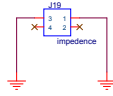
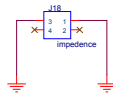
HS2



PCIE1



PCIE2



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Size	Document Description	Rev
Custom	MECH	6.0

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VR THERMAL PROTECTION

